Flexibility in MLVR-VSC back-to-back link

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Abstract

This thesis describes the flexible voltage control of a multi-level-voltage-reinjection voltage source converter. The main purposes are to achieve reactive power generation flexibility when applied for HVdc transmission systems, reduce dynamic voltage balancing for direct series connected switches and an improvement of high power converter efficiency and reliability. Waveform shapes and the impact on ac harmonics caused by the modulation process are studied in detail. A configuration is proposed embracing concepts of multi level, soft-switching and harmonic cancellation. For the configuration, the firing sequence, waveform analysis, steady-state and dynamic performances and close-loop control strategies are presented.

In order not to severely compromise the original advantages of the converter, the modulated waveforms are proposed based on the restrictions imposed mathematically by the harmonic cancellation concept and practically by the synthesis circuit complexity and high switching losses. The harmonic impact on the ac power system prompted by the modulation process is studied from idealistic and practical aspects.

The circuit topology being proposed in this thesis is developed from a 12-pulse bridge and a converter used classically for inverting power from separated dc sources. Switching functions are deduced and current paths through the converter are analysed.

Safe and steady-state operating regions of the converter are studied in phasor diagrams to facilitate the design of simple controllers for active power transfer and reactive power generations. An investigation into the application of this topology to the back-to-back VSC HVdc interconnection is preformed via EMTDC simulations.

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Glossary

Abbreviations and Acronyms

AC-DC	Alternating Current-Direct Current
BTB-VSC	Back To Back-Voltage Source Converter
CSC	Current Source Converter
EMT	Electromagnetic Transient
ESEDS	Error Square Error Derivative Square
FACTS	Flexible alternating current Transmission System
GCT	Gate Commutated Turn-Off Thyristor
GTO	Gate Turn Off thyristors
HVdc	High Voltage direct current
HVdc-VSC	High Voltage direct current-Voltage Source Converter
IEGT	Injection Enhanced Gate Transistor
IGBT	Insulated Gate Bipolar Transistor
IGCT	Insulated Gate Commutated Turn-Off Thyristor
MLCC-VSC	Multi Level Capacitor Clamped-Voltage Source Converter
MLDC-VSC	Multi Level Diode Clamped-Voltage Source Converter
MLGB-VSC	Multi Level Generalised Bi-logic-Voltage Source Converter
MLVR-VSC	Multi Level Voltage Reinjection-Voltage Source Converter
MLVSC	Multi Level Voltage Source Converter
NPC	Neurtral Point Clamped
p.u.	per unit
PLO	Phase Locked Oscillator
PSCAD/EMTDC	Power System Computer Aided Design/Electromagnetic Transient with direct current
PWM	Pulse Width Modulation
PWM-CSC	Pulse Width Modulation-Current Source Converter
PWM-VSC	Pulse Width Modulation-Voltage Source Converter
SHE	Selective Harmonic Elimination
SPWM	Sinewave-Pulse Width Modulation
SSSC	Solid State Series Controller

STATCOM	Static Compensator
SVC	Static Var Compensator
THD	Total Harmonic Distortion
UPFC	Unified Power Flow Controller
VCO	Voltage Controlled Oscillator
VSC	Voltage Source Converter
ZVS	Zer Voltage Switching(ed)

Symbols

a	MLVR-VSC interface transformer transformation ratio
$a_{Y/Y}$	Turns ratio of the Y/Y configured interface transformer
$a_{Y/\Delta}$	Turns ratio of the Y/Δ configured interface transformer
A_{Yk}	Amplitude of cosine components of the Y/Y main bridge dc side voltage
$A_{\Delta k}$	Amplitude of cosine components of the Y/Δ main bridge dc side voltage
C_1	Y/Δ main bridge main dc capacitor
C_2	Y/Y main bridge main dc capacitor
C_H	H-bridge capacitor
D	Depth of the modulation notch on the MLVR-VSC dc side voltage
E	Width of the highest and lowest steps of the reinjection voltage
I_A	Phase A MLVR-VSC ac output current
I_{A1}	Phase A fundamental component amplitude of the MLVR-VSC ac output current
I_{An}	Phase A nth order harmonic component amplitude of the MLVR-VSC ac output current
I_{Arated}	Rated phase A MLVR-VSC ac current
I_{ARMS}	Phase A RMS current of the MLVR-VSC ac output current
I_{dc}	MLVR-VSC dc load current
I_o	MLVR-VSC ac output current vector
I_r	Current flow through the reinjection branch
I_{SR}	Rated line current
I_{Ydc}	Dc side current of the Y/Y main bridge
$I_{\Delta dc}$	Dc side current of the Y/Δ main bridge
k	Operating Index of the MLVR-VSC

L_l	Leakage inductance of the MLVR-VSC interface transformer
m	Level number of the Reinjection Voltage
$N_{capacitor}$	Number of capacitor utilised in a MLVSC
N_{diode}	Number of diode utilised in a MLVSC
N_{valve}	Number of valve utilised in a MLVSC
P	Active power
Q	Reactive power
S	Apparent power
S_{SR}	Rated apparent power
THD_I	Total harmonic distortion of the MLVR-VSC ac output current
THD_V	Total harmonic distortion of the MLVR-VSC ac output voltage
V_1	Voltage fundamental component amplitude
V_A	Phase A MLVR-VSC ac output voltage
V_{A1}	Phase A fundamental component amplitude of the MLVR-VSC ac output voltage
V_{An}	Phase A nth order harmonic component amplitude of the MLVR-VSC ac output voltage
V_{ARMS}	Phase A RMS voltage of the MLVR-VSC ac output voltage
V_{C1}	Voltage across Y/Δ main bridge main dc capacitor
V_{C2}	Voltage across Y/Y main bridge main dc capacitor
V_{cosYan}	nth order harmonic component of the Y/Y main bridge ac output caused by cosine components of dc side voltage
$V_{cosΔan}$	nth order harmonic component of the Y/Δ main bridge ac output caused by cosine components of dc side voltage
V_{dc}	DC bus voltage
V_{dcYan}	nth order harmonic component of the Y/Y main bridge ac output caused by constant dc side voltage
$V_{dcΔan}$	nth order harmonic component of the Y/Δ main bridge ac output caused by constant dc side voltage
V_l	Voltage for one step level on the dc side
V_{Lr}	Voltage across the inductor residing on the reinjection branch
V_o	MLVR-VSC ac output voltage vector
V_r	Reinjection voltage
V_S	AC source voltage
V_{SR}	Rated phase voltage
V_{Srated}	Rated power system source voltage

V_{sync}	Grid synchronising signal obtained from the PLO unit
V_{YA}	Phase A output voltage of the Y/Y main bridge
V_{YY}	Dc side voltage across the Y/Y main bridge
$V_{Y\Delta}$	Dc side voltage across the Y/Δ main bridge
$V_{\Delta A}$	Phase A output voltage of the Y/Δ main bridge
W	Width of the modulation notch on the MLVR-VSC dc side voltage
W_l	Step width for one step level on the dc side
x_l	per unit value of MLVR-VSC interface transformer leakage reactance (fundamental frequency)
X_l	Leakage reactance of the MLVR-VSC interface transformer (fundamental frequency)
Z_{base}	Base impedance of the rated MLVR-VSC
ϕ	Phase angle difference between ac source and VSC output voltage
θ	Power angle of the MLVR-VSC

Chapter 1

Introduction

1.1 Converter for Transmission Level Application

Power electronics was first applied to power systems with the advent of power semiconductor diodes and thyristors through the application of High Voltage dc (HVdc) transmission systems. However, the uni-directional current capability of early naturally-commutated thyristor bridges only allows the implementation of converters which absorb reactive power. Later developed self-commutated devices such as Gate-Turn-Off thyristors (GTOs) and Insulated-Gate-Bipolar-Transistors (IGBTs) have advanced capabilities to force turn-off and carry bi-directional currents through their anti-parallel diode connections. Hence, a new type of four-quadrant converter based on voltage source (VSC), which has been successfully applied to a large number of power conversion problems at low and medium levels, was developed.

Adopting VSC solutions to power transmission, however, has to overcome issues typically related to high voltage levels and low efficiency. Although the capacity of power semiconductor devices has gradually increased, high voltage ratings still require combining devices in series. These series connected power switch valves can be fired either synchronously or asynchronously.

Synchronous control is used in two level schemes and presents problems like imbalance voltage stress across individual devices and high *dV/dt* induced on the valves. Realistically, the power semiconductors in a series chain will not acquire perfectly similar characteristics. While during static operation, the voltage across each device can be clamped with very large identical resistors, the dynamic voltage balancing is a more difficult problem. The switch that turns off first or turns on last will have to sustain the entire voltage stress of the series chain. Additionally, full voltage changes within a few microseconds, i.e. a *dV/dt* higher than 1-10GV/s will cause serious electromagnetic interference and possibly components insulation damage.

The asynchronous control is used in multi-level schemes to improve the voltage balancing under dynamic conditions while the steady-state equal voltage sharing is achieved with the assistance of switching device voltage clamping. The output waveforms with multi levels have reduced harmonic content and incur much lower *dV/dt* stress on the switches. Unfortunately, the different multi-level VSC (MLVSC) configurations which have been proposed [11, 18 & 38] require the number of circuit elements to increase sharply as the level number increases. Moreover, the multi-level diode clamped VSC (MLDC-VSC), being the most prominent multilevel configuration among those proposed, encounters difficulties caused by capacitor voltage imbalance [48]. The level number is limited to a relative low value, which results in the use of Pulse Width Modulation (PWM) techniques to suppress the harmonics further.

The multi-level-voltage-reinjection VSC (MLVR-VSC) was conceived by Arrillaga et. al. [22] for handling transmission level conversions. The harmonic cancellation concept, which the MLVR-VSC relies heavily upon, provided a feasible converter which outputs good quality waveforms and avoids issues such as dynamic voltage balancing and high switching losses. The dc side waveform functions which were derived to cancel most of the ac side harmonics also provided zero voltage commutation conditions to the ac main bridges. Multilevel technology has been adopted to generate the dc side waveforms and reduce the *dV/dt* stress in the circuit.

1.2 Objective of Reactive Power Generation Flexibility in HVdc-VSC

Fundamental frequency switching of the 12-pulse converter bridge switches in the MLVR-VSC eventually limits the controllability of the output voltage. Originally, the only controllable parameters were the dc bus voltage, V_{dc}, and the phase angle difference, ϕ, between the output voltage waveform and the power system voltage waveform. When the 12-pulse converter bridge is not controlled by a PWM or Selective Harmonic Elimination (SHE) pattern designed for harmonic elimination, output voltage control is obtained by varying the dc bus voltage through ϕ angle control. This is achieved by charging or discharging the dc capacitor. Consequently, the dynamic response depends upon the dc capacitor value, the dc voltage and the ac inductor [17].

The link between the 12-pulse converter bridge in an MLVR-VSC and the power system is made through two sets of interface transformers, one having a Y/Y winding configuration while the other has a Y/Δ winding configuration. Under balanced condition, the power flow into the MLVR-VSC can be simplified to a per phase basis. Assuming the ac busbar voltage to be perfectly sinusoidal, the average power transfer between the MLVR-VSC and the ac system only involves the fundamental components. The simplified model consists of an ideal interface transformer with fundamental leakage reactance linking two voltage sources, one being the ac busbar voltage with the other being the MLVR-VSC fundamental ac output component as shown in figure 1.1.

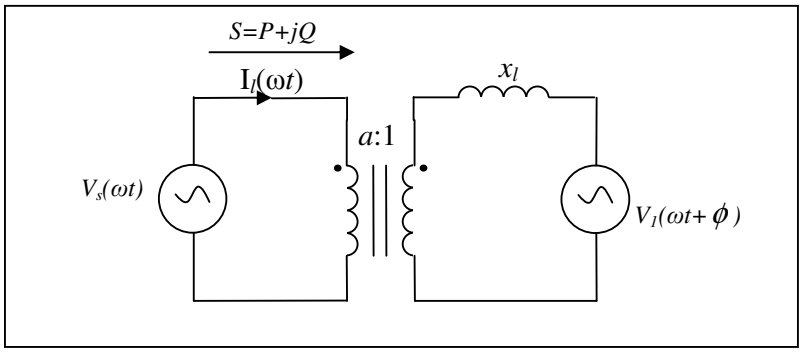


Figure 1.1 Simplified per phase model of the MLVR-VSC connected to the ideal ac system.

In an HVdc back-to-back application, any variation of the dc bus voltage will be reflected onto both converters. This signifies that changing the active and reactive power flows of one end will eventually affects those of the other end. This limitation in controllability is the result of the fact that the MLVR-VSCs share the same dc bus voltage and their corresponding switches in the main bridges operate at fundamental frequency.

If both power systems which the HVdc transmission system links together are identical, the operation condition dependence of one side converter to the other would not be an issue. However, this is never the case practically and hence they require different reactive power compensations to reduce I^2R losses and uphold busbar voltage. An extreme case would be one converter (usually the rectifier station) in the proximity of generating stations while the other side is connected to passive loads covering a large area. Therefore, it would be convenient and economical to be able to control each converter reactive power independently.

The converter cable is designed to carry only 1 p.u. rated current which implies that the converter can only supply or absorb reactive power of 1 p.u. Assuming no fault conditions, maximum (1 p.u.) reactive power flexibility in the MLVR-VSC operation can be achieved by varying the fundamental component by as much as the interface transformer leakage reactance in p.u. value. This can be proven by

$$S = I_l V_S = \frac{(V_S - V_1)V_S}{jx_l} = \frac{[-j(V_S - V_1\cos\phi) + V_1\sin\phi]V_S}{x_l} \tag{1.1.1}$$

$$P = \frac{V_S V_1 \sin\phi}{x_l} \tag{1.1.2}$$

$$Q = \frac{V_S{}^2 - V_S V_1 \cos\phi}{x_l} \tag{1.1.3}$$

where x_l is the fundamental leakage reactance of the interface transformer in per unit value and variables are defined as shown in figure 1.1.

$$\frac{\partial Q}{\partial V_1} = \frac{V_S \cos\phi}{x_l} \tag{1.1.4}$$

Assuming V_S = 1 p.u. and maximum reactive flexibility, $\phi = 0 \rightarrow \cos\phi = 1$

$$\frac{\partial Q}{\partial V_1} = \frac{\cos\phi}{x_l} = \frac{1}{x_l} \tag{1.1.5}$$

$$\Delta Q = \frac{\partial Q}{\partial V_1}\Delta V_1 = \frac{\Delta V_1}{x_l} \tag{1.1.6}$$

If ΔQ=1 p.u.

$$\Delta V_1 = x_l \tag{1.1.7}$$

There are two alternatives to acquire freedom of the dc voltage relationship with the ac voltage output in an HVdc back-to-back transmission system. One converter ac component amplitudes relationship with the dc bus voltage can be changed directly by modifying its ac output waveform shapes. This technique will modulate the MLVR-VSC voltage fundamental component and requires more frequent switching events on the 12-pulse converter bridge. Alternatively, multiple output voltage vectors with

different phase angles can be implemented with multiple converters parallel connected on one terminal. Their resultant vector can be freely controlled by changing these phase angles.

This thesis is concerned with the MLVR-VSC reactive power flexibility obtained through the fundamental component amplitude modulation method.

1.3 Thesis Outline

Chapter 2 reviews the historical development of the MLVR-VSC, along with the harmonic cancellation concept derived by Liu [24] in an attempt to minimise the MLVR-VSC ac harmonic content. Features and applications of MLVR-VSC are given in order to highlight its outstanding advantages over the PWM based VSCs. A method to achieve reactive power flexibility is presented with its basic concepts and implications on the MLVR-VSC.

Chapter 3 analyses the harmonic performance of the modulated MLVR-VSC waveforms and provides explanations of the waveform shapes used. Practical issues such as the finite quantisation level and non-homogenous step width are investigated for their impact on the ac side harmonic performance.

The main objective of chapter 4 is to present the circuit topology and the switching functions used to embrace the fundamental component modulation into the MLVR-VSC. Ac and dc current paths following the modulation process are also mentioned.

Chapter 5 develops the control model and system of an HVdc link built with two MLVR-VSCs in back-to-back configuration. The operation regions and safety margins of the HVdc link are studied using phasor diagrams composed from fundamental components of the MLVR-VSCs and the power systems. At the end of the chapter, simulation results obtained from the PSCAD/EMTDC simulation platform are presented.

Finally, chapter 6 summarises this research and discusses the possibilities for future work.

Chapter 2

Operating Principles of MLVR-VSC

2.1 Introduction

The reinjection conversion concept proposed by Arrillaga et. al. [23] is adopted in this thesis. It offers the advantages of low harmonic distortion and soft-switchings, hence it is very attractive for high power applications. Simulation studies in PSCAD-EMTDC have proven the functionality of VSCs based on this concept in both Static Compensator (STATCOM) and HVdc back-to-back applications [24]. A further enhancement of the converter is to embrace the function of independent reactive power generation controls for an HVdc-VSC application. This flexibility will allow the converter to be broadly applied and will rival the PWM based converters.

The first sections in this chapter present a summary of chronological events associated with the development of the reinjection concept. Basic concepts and the applied technology of VSCs are also introduced. Compared with the thyristor based converters, VSCs have better transient performance and more applicable quadrants in the power circle. These sections served as a prelude for the subsequent sections and chapters.

The current trend of ac transmission system is that many Flexible AC Transmission System (FACTS) applications previously implemented with thyristor based converter are slowly changing to VSCs, especially those incorporating the 12-pulse converter bridge. For introductory purpose, the basic operation principal of the 12-pulse converter bridge and the harmonic cancellation concept is briefly mentioned. Appendix A documents more mathematical details of this concept.

In order to demonstrate the distinct advantages of the converter proposed, section 2.4 is included and section 5 summarises the observations made from simulation results presented in reference 24. Lastly, a method is proposed to facilitate reactive power generation flexibility in HVdc-VSC applications. Its basic concepts and implications on high voltage converter application are presented. The work mentioned in chapters

subsequent to this is based on the aim to gain reactive power flexibility through the waveform modulation method.

2.2 Background Information

2.2.1 Historical Background

Currently, line-commutated thyristor-based converters are preferred in high power applications. A 1.4GW application can be found in reference 42. An active ac source has to be present to drive the thyristor valve commutations because the thyristors do not have turn-off capability. In the inverter mode of operation, commutation failure is a common problem [13]. On the other hand, self-commutated converters are proposed for somewhat lower power capacity, 80MVA for Gate-Commutated Turn-Off Thyristors (GCT) and 8MVA for Injection-Enhanced Gate Transistor (IEGT) [2]. Self-commutated devices based on VSCs can operate in all four quadrants of the power circle and their switch commutations can be independent of ac source. However the development of self-commutated switches has not been able, as yet, to match the power ratings of thyristors.

Series connection of self-commutated switches is not a preferred solution in the industry due to complications such as static balancing, dynamic balancing and high dynamic voltage (dV/dt) stress. In 2002, Liu proposed a new type of voltage source converter [23], which has the potential of solving these difficulties by embracing multi-level and soft-switching concepts.

The concept of *harmonic injection* was first proposed by Bird [8] in 1969 and further generalised by Ametani in 1972 [3]. In his paper, Bird used third harmonics to modify the rectifier current waveform in order to reduce the ac side current harmonic content. Ametani concluded that the third harmonic was the most suitable general purpose injection current, and that the ninth harmonic was most appropriate for the reduction of the higher order harmonics. Despite the appealing advantage of a good quality output waveform, the work on building a prototype was impeded by control difficulties in frequency, amplitude and phase using technology known at that time. The development of this idea eventually halted.

In was not until 1980 that Baird and Arrillaga [5] revived the concept of harmonic injection by bringing it to an applicable stage. Extra components, mainly power

switches, were added to synthesize a step varying waveform to approximate the required harmonic current injection and employed the dc side ripple voltage to realise the natural commutation for the extra power switches. Under the new scheme, the dc ripple voltage is re-rectified and added to the dc output to improve the dc output voltage waveform. It was given the name of "*dc ripple injection*".

Villablanca and Arrillaga brought the concept of dc ripple reinjection a step further by introducing multi-level into the scheme. The amplitude of the multi-level reinjection current is matched to the operating conditions, the frequency and phase are synchronised with the power supply. Thyristors are added to synthesize the reinjection ripples and they commutate naturally. Based on the fixed amplitude relation between the dc current and the reinjection current, the optimum harmonic reduction for all the operation is ensured. 12-pulse, 18-pulse, 24-pulse, 36-pulse and 48-pulse equivalent high pulse conversion have been demonstrated [39-45].

In Villablanca's work, the reinjection waveform was determined without theoretical explanation and mathematical evidence. Phasor diagram and graphical interpretation were used [39-45]. The lack of mathematical explanation has made the optimisation of the reinjection waveform for harmonic cancellation a difficult and cumbersome task. In light of this short-coming, Liu first derived the Fourier components of a general 12-pulse converter bridge [24] and he concluded that the dc reinjection waveform should operate at six times the fundamental frequency of the ac system. After the ideal reinjection waveform which has an output of zero Total Harmonic Distortion (THD) was derived, he then optimised the *error square-error derivative square* (ESEDS) symmetrical waveform with respect to the ideal reinjection waveform. This ESEDS-symmetrical waveform can be closely approximated by a triangular waveform for simplification in implementation of high number of level (typically more than 5 levels) [24]. Also, in Liu's work, the dc reinjection scheme has improved thyristor-based line-commutated based systems to self-commutated IGBTs or GTOs based systems. Consequently, the dc reinjection concept originally adopted for inverter operation has evolved into a four quadrant converter. Liu named this converter the *Multi-level Reinjection AC-DC Converter*. It should be noted that in section 2.3, the harmonic cancellation concept is targeted at VSC. However, the Current Source Converter (CSC) can be viewed as the counterpart of VSC and that the general mathematical expressions and waveforms characteristics apply equivalently. For the VSC version, when combined with dc multi-level reinjection, it is named as *Multi-level Voltage Reinjection-Voltage Source Converter* (MLVR-VSC).

2.2.2 Technical Background

As the development of power electronics technology continues, the emergence of four quadrant VSCs, which are based on controllable switches such as GTOs and IGBTs, have replaced the conventional Static VAR Compensators (SVCs) as a more promising reactive compensation with better transient handling capability and a fraction of the footprint of the SVCs. Significant improvements have been made to these switches with higher power handling and lesser switching losses; leading to higher switching frequencies.

In ac-dc power converters that use fully controllable semiconductors rather than conventional thyristors, the dc input can be either a voltage source (typically a capacitor) or a current source (typically a voltage source in series with an inductor). With reference to this basic operational principal, converters can be classified as either voltage source (VSC), or current source (CSC). For economic and performance reasons, most reactive power controllers are based on the VSC technology. VSC has become the basic building block of the new generation of power electronics controllers that have emerged from the FACTS and custom power initiatives [13]. Amongst various worldwide operations, the most popular are: - STATCOMs, solid-state series controllers (SSSCs), unified power factor controllers (UPFCs) and HVdc-VSCs [10].

There are several VSC topologies currently in use in actual power system operation and some others that hold great potential, including: the single-phase full bridge (H-bridge), the conventional three-phase, two-level converter, and the three-phase, three-level converter based on the neutral-point-clamped converter. Other VSC topologies are based on the combinations of the neutral-point-clamped (NPC) topology and multi-level-based systems. Common aims of these topologies are: *to minimised the operating frequency of the semiconductors inside the VSC and to produce a high-quality sinusoidal voltage waveform with minimum or no filtering requirements* [37].

Under the general analysis of VSC, the dc link voltage can be assumed constant and the corresponding ac voltage is chopped, consisting of one (fundamental switching) or more pulse per half period (PWM). The dc bus voltage polarity does not reverse, therefore the dc voltage across the switches remains of the same polarity. The dc currents through the switches however can reverse their direction instantaneously. The switches are therefore of bidirectional current, uni-directional voltage blocking capability; IGBTs and asymmetrical GTOs have this feature. Capacitors or an energy

storage device such as batteries can be used as the dc source. If the switches are synchronised with the ac supply voltage, the VSC can be viewed as a *static synchronous generator*, with features similar to those of a synchronous machine or synchronous condenser.

2.3 Harmonic Cancellation Concept

2.3.1 Basic Operation of 12-pulse Converter Bridge

In the MLVR-VSC, a 12-pulse converter bridge, which consists of two three-phase full-bridges and two interface transformers (Y/Y and Y/Δ connected), is used. In order to cancel the harmonics of order $n=6(2l-1)\pm1$ ($l=1,2,3,\ldots$), the secondary to primary windings turn ratio of the Y/Δ interface transformer must be $1/\sqrt{3}$ times of that of the Y/Y interphase transformer. Figure 2.1 shows the schematic of a 12-pulse converter bridge.

A 180° (half period of the fundamental cycle) switching pattern is used in all the six legs of the 12-pulse converter bridge under the general firing control strategy of the MLVR-VSC. Each arm is synchronised with respect to their corresponding phase voltage on the primary side. Figure 2.2 shows the switching pattern used for the 12-pulse converter bridge.

Assuming a simplified case where constant dc voltage is applied to the bridges, i.e. $V_{YY}(\omega t)=V_{Y\Delta}(\omega t)=V_{dc}$, the output waveform on one particular phase, say phase A, during balance operation is as shown in figure 2.3.

The Fourier analysis of the phase A primary winding voltages, V_{YA} and $V_{\Delta A}$, shown in figure 2.3 yields harmonics of order $n=(6l-1)\pm1$, as in

$$V_{dcYAn}=\frac{4\left[1-(-1)^n\right]}{3n\pi}\frac{V_{dc}}{2}\cos^2\left(\frac{n\pi}{6}\right)\times a_{Y/Y} \qquad (2.3.1.1)$$

$$V_{dc\Delta An}=\frac{2\left[1-(-1)^n\right]}{n\pi}\frac{V_{dc}}{2}\cos\left(\frac{n\pi}{6}\right)\times a_{Y/\Delta} \qquad (2.3.1.2)$$

where $a_{Y/Y}$ and $a_{Y/\Delta}$ are the secondary to primary windings turn ratio of the Y/Y and Y/Δ interface transformers respectively.

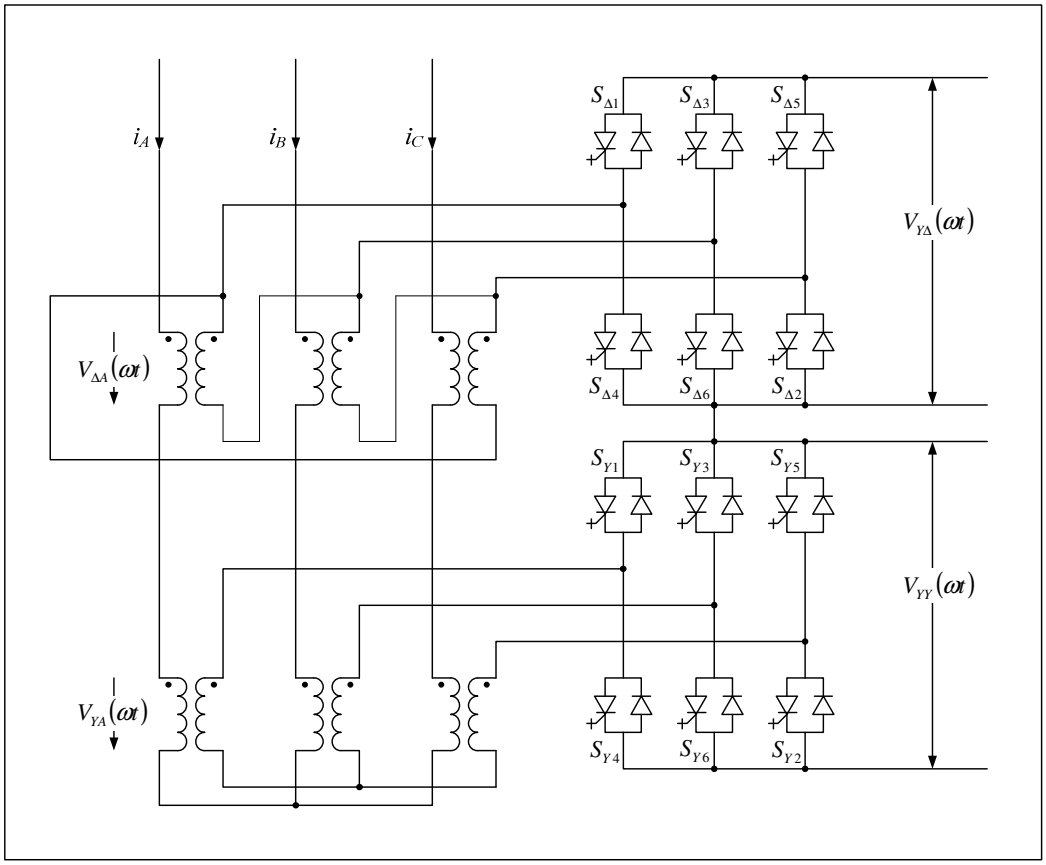


Figure 2.1 Schematic of a 12-pulse converter bridge based on self-commutated switches.

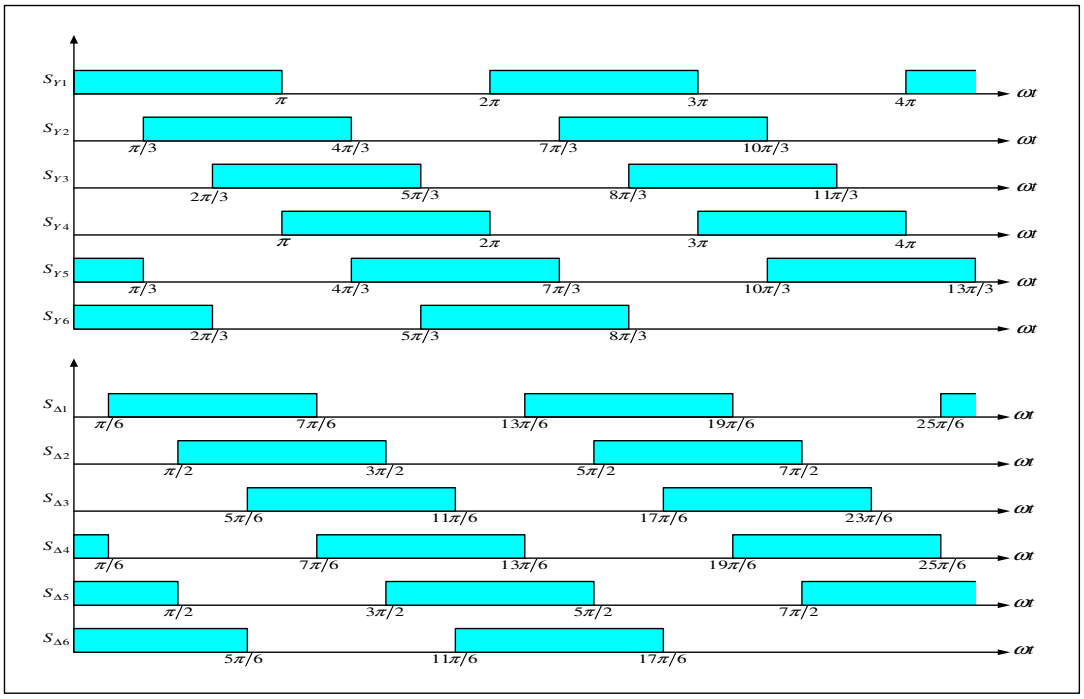


Figure 2.2 Switching functions of a 12-pulse converter bridge.

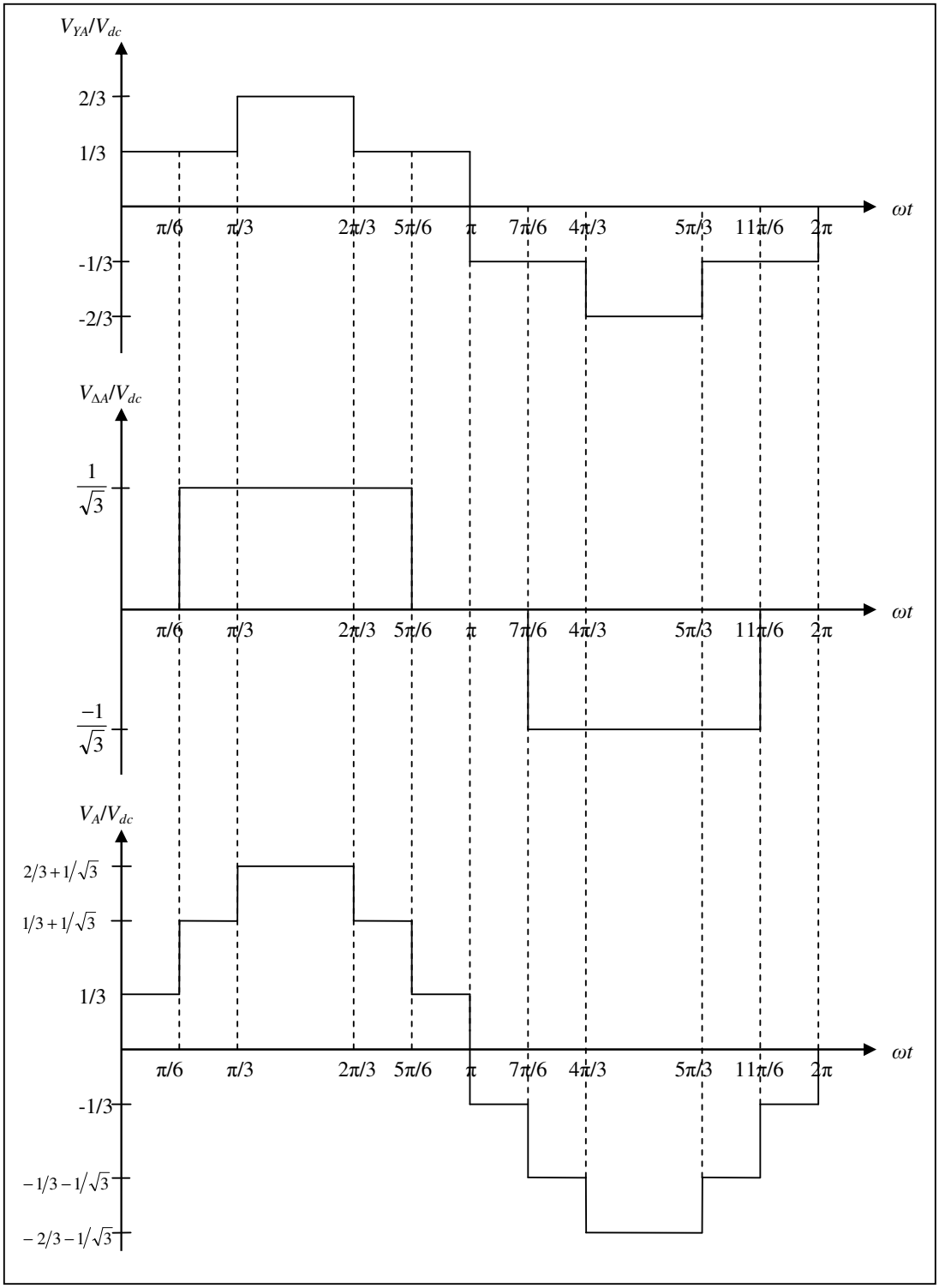


Figure 2.3 Output phase voltage for 12-pulse converter bridge with constant V_{YY} and $V_{Y\Delta}$.

The Y/Y interface transformer output harmonics of order n=6(2l-1)$\pm$1 are in phase with the fundamental component while the harmonics of same order on the Y/Δ interface transformer output are 180° phase shifted from the fundamental component. Provided that both transformers have equal voltage ratios, series connection of the interface transformer primary windings will cause these harmonics to cancel out each other. The harmonic's angles of order n=12$l\pm$1 for both the interface transformer primary outputs are in phase, hence they will add constructively and penetrate into the ac system if left alone. The objective of the *dc reinjection* is to inject the corresponding harmonics on the dc side which will cancel these remaining harmonics caused by the constant dc source.

2.3.2 Principle of DC reinjection

The 12$l\pm$1 harmonics caused by the constant dc voltage can be cancelled by injecting harmonics which are in-phase with the fundamental component at the dc bus voltage. It has been shown [24] that these harmonics have to be multiples of six times the fundamental frequency. Out-of-phase components must be avoided because they induce even order harmonics, which cannot be cancelled by the 12-pulse bridge operation, on the ac side.

Let the dc voltages now contain a constant dc average value with some ripples. They can be written as

$$V_{YY}(\omega t)=\frac{V_{dc}}{2}+\sum_{k=1}^{\infty}A_{Yk}\cos(6k\omega t) \tag{2.3.2.1}$$

$$V_{Y\Delta}(\omega t)=\frac{V_{dc}}{2}+\sum_{k=1}^{\infty}A_{\Delta k}\cos(6k\omega t) \tag{2.3.2.2}$$

The corresponding harmonics on the ac side caused by the reinjection harmonics, $\sum_{k=1}^{\infty}A_{Yk}\cos(6k\omega t)$ and $\sum_{k=1}^{\infty}A_{\Delta k}\cos(6k\omega t)$ are

$$V_{\cos YAn}(k)=\frac{4n\left\lfloor 1-(-1)^{n}\right\rfloor}{3\pi\left(n^{2}-36k^{2}\right)}A_{Yk}\cos^{2}\left(\frac{n\pi}{6}\right)\times a_{Y/Y}\qquad (k=1,2,3\ldots) \tag{2.3.2.3}$$

$$V_{\cos\Delta An}(k)=\frac{2n(-1)^{k}\left\lfloor 1-(-1)^{n}\right\rfloor}{\pi\left(n^{2}-36k^{2}\right)}A_{\Delta k}\cos\left(\frac{n\pi}{6}\right)\times a_{Y/\Delta}\quad (k=1,2,3\ldots) \tag{2.3.2.4}$$

Magnitudes of A_{Yk} and $A_{\Delta k}$ are solved by matching equation 2.3.2.3 to 2.3.1.1 and equation 2.3.2.4 to 2.3.1.2. It involves solving infinite series of A_{Yk} and $A_{\Delta k}$ to each specific harmonics on the ac side as shown in

$$\sum_{k=1}^{\infty} \frac{A_{Yk}}{(12l \pm 1)^2 - 36k^2} = \frac{V_{dc}}{2(12l \pm 1)^2} \qquad (l=1,2,3,\ldots) \qquad (2.3.2.5)$$

$$\sum_{k=1}^{\infty} \frac{(-1)^k A_{\Delta k}}{(12l \pm 1)^2 - 36k^2} = \frac{V_{dc}}{2(12l \pm 1)^2} \qquad (l=1,2,3,\ldots) \qquad (2.3.2.6)$$

Additionally, the condition of $(-1)^k A_{\Delta k} = A_{Yk}$ (k=1,2,3,…) has to be fulfilled so that harmonics of order $n=6(2l-1)\pm 1$ (l=1,2,3,…) will be cancelled out by the 12-pulse bridge operation. Therefore, the solution for harmonic reinjection on the dc side is reduced to equation 2.3.2.5.

2.3.3 Symmetrical Reinjection

The resolved reinjection harmonics in equation 2.3.2.1 and 2.3.2.2 can be graphically interpreted as parts of a sine wave (0° to 30° and 150° to 180°) repeated six times with a dc offset in a fundamental cycle, as shown in figure 2.4. When the waveforms of $\sum_{k=1}^{\infty} A_{Yk} \cos(6k\omega t)$ and $\sum_{k=1}^{\infty} A_{\Delta k} \cos(6k\omega t)$ are summed together, they will yield a waveform with a zero offset and some ripples. Practically, it is difficult to synthesize any ripples on the dc side. Hence, a simplified approximation is needed.

Two approximations have been proposed by Liu [24]. Because sin(α) can be approximated to α and –α for values of 0°<α<30° and 150°< α<180°, the reinjection waveform can be approximated as a linear triangle repeated six times in a fundamental cycle. The reinjection based on linear triangular waveforms is named as the *linear reinjection*. The other approximation is derived by *minimising the integration of the error square and the derivative square* compared to the sine wave partitions. Liu had derived an explicit formula that will yield lesser ac harmonic content than the linear reinjection. However, the cost of this slightly better harmonic performance is that the waveform is non-linear. Liu named this approximation as *error square and error derivative square* (ESEDS). The voltage THDs for both the ideal linear reinjection and ESEDS reinjection are 1.0553% and 1.0168% respectively.

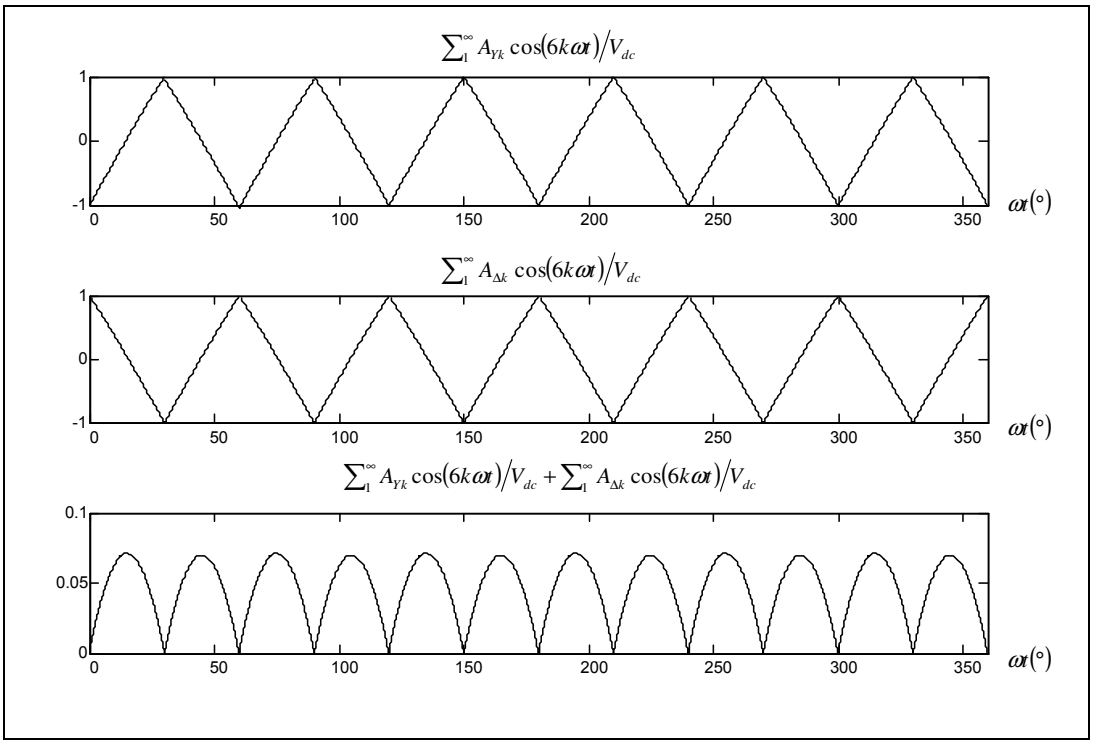


Figure 2.4 Reinjection harmonics normalised against dc bus voltage, V_{dc}.

Regardless which symmetrical approximation is used, it is possible to synthesize the reinjection harmonics (although with different difficulties). The dc side voltages, $V_{Y\!Y}(\omega t)$ and $V_{Y\!\Delta}(\omega t)$, now consist of a constant dc voltage and reinjection harmonics. Their waveforms possess the following characteristics:

- Zero values appear at the points where the switches in the 12-pulse converter bridge commutate;
- The derivatives of the waveform are limited; particularly around the zero values where the power switches change their states;
- The two waveforms, $V_{Y\!Y}(\omega t)$ and $V_{Y\!\Delta}(\omega t)$, add to a constant dc level.

2.4 Features of MLVR-VSC

2.4.1 Stepped waveforms

The varying dc waveforms presented in the previous sections have to be quantified into discrete levels before they can be synthesised by any circuit. The ESEDS explicit formula requires that the step levels have unequal heights. Liu demonstrated that these

non-linear step levels can be generated by adding and subtracting isolated ac voltage sources to the dc voltage of the two main bridges. However, the need for isolation requires the use of reinjection transformers with rigid winding restrictions. It is only practically feasible for very low level numbers, $m<5$. Any further increase in m will require custom-made reinjection transformers with turn ratios which are difficult to achieve. In addition, the ESEDS waveforms do not provide true zero voltages for the main bridge commutations.

The triangular waveforms in the linear reinjection concept can be equally quantified. This makes a high level number configuration possible by adopting asynchronous valves control, i.e. multi-level scheme, to yield a controllable voltage divider to generate the voltage step levels. Generally, the controllable voltage divider consists of a series of capacitor-clamped switches. Because it is difficult to precisely control the individual voltages of each capacitors, multi-level topologies are more suited for linear reinjection waveforms synthesis, i.e. identical level heights. There are many topologies already available in the literature [11, 18 & 38] which can be implemented to synthesize the linear reinjection waveforms. Appendix B briefly discusses the operations, advantages and limitations, in association with the reinjection concept, of these topologies.

It is obvious that a higher level number, regardless of ESEDS or linear reinjection, results in lesser harmonic contents on the ac output. Also, due to the step-by-step nature of the varying dc waveforms, the higher level number used will induce lesser *dV/dt* stress on the main bridge switches. In table 2.1, the ac output THDs for the ESEDS and linear reinjections of each level number are listed. It can be seen that the THDs do not reduce much after $m>8$ and that the harmonic performance of the linear reinjection is not much poorer than the ESEDS reinjection when the level number is high enough. Also, the linear reinjection will provide true zero voltage periods for the main bridge commutations while the ESEDS reinjection only approximates the zero values to a very small voltage drop. For these reasons, the voltage source converter proposed in this thesis will adopt the linear reinjection scheme with multi-level topology.

Table 2.1 THD of the discrete ESEDS and linear reinjections [24].

Level m	3	4	5	6	7	8	9	10
THD_{ESEDS} (%)	5.09	3.88	3.16	2.69	2.36	2.13	1.95	1.81
THD_{lin} (%)	7.77	5.25	3.99	3.28	2.77	2.45	2.20	2.02

2.4.2 Soft-Switching

Soft-switching implies that the condition at which the commutation of the power electronics switches occur to be zero-voltage or zero-current. This method has the advantages, over traditional "hard-switching", of reduced power dissipation during switching intervals, while at the same time eliminating much of the generated radio frequency energy, or high frequency "noise" [15]. From literature reviews [9, 14, 15 & 46], most of the techniques used to achieve the soft-switching condition make use of the resonant techniques to soften the switching transition.

Resonant elements (either inductors or capacitors) which are placed on the main current conduction paths will incur high switch voltage stress and conduction loss due to high circulating energy. The energy stored in these elements is sensitive to power conditions, thus limiting the soft-switchings to a narrow load range. Auxiliary resonant networks, on the other hand, will add to component cost by having auxiliary switches, which are not soft-switched, to activate the networks during switching transition and deactivate them after. The switching losses involved in the operation of the auxiliary networks are typically lower than those of a PWM converter. [15]

In the MLVR-VSC, soft-switching is achieved without any additional resonant circuits employed. Having the periodic dc side waveforms synchronised to six times the fundamental frequency of the ac system, the switches in the main converter bridge commutate during the periods when voltage (for VSCs) or current (for CSCs) levels across the 6-pulse converter bridge are zero. The duration of these zero voltage levels can be actively controlled (with some impact on the harmonic performance), hence soft-switchings can be preserved for any loading condition of the converter. No additional conduction loss and component cost or complicated electromagnetic studies of the switching devices are necessary as in the case with resonant method based soft-switchings.

With the currently available voltage and turn-off current ratings, self-commutated semiconductor devices are not sufficient to meet the requirement of high power applications on an individual basis. Very often, these devices are series connected to allow using such devices in high voltage applications. Methods which help to acquire equal voltage sharing amongst the devices in the series chain are broadly categorised into load side and gate side approaches. Load side approach with passive or active snubbers is obtained at the cost of slower switching frequency and higher power loss

[6 & 34]. Voltage sharing using actively controlled gate signals has been proposed for field effect devices [7].

Under zero-voltage switching (ZVS), the problem of dynamic voltage sharing of direct series connected self-commutated power switches is eliminated for the 12-pulse main bridges. Simple snubber circuits are possible for main bridge valves in the MLVR-VSC to obtain static voltage sharing and the parasitic energies can be recovered. The risk of short-circuit on the dc side due to commutation in the main bridge is also eliminated and hence, there is no need for a time delay between switching off one of the valves in the same pole or phase-leg while switching on another.

2.5 Application of MLVR-VSC

MLVR-VSC promises many advantages unavailable to thyristor based converters and many VSCs. In particular, MLVR-VSC is more attractive in high power applications, whether it is FACTS or HVdc, due to its advance features of low THD, ability to convert real power and generate reactive power and soft-switching. Two main possible areas of application for the MLVR-VSC are the STATCOM and the back-to-back HVdc.

2.5.1 STATCOM

The STATCOM is the static counterpart of the rotating synchronous condenser (using a synchronous machine) but with a faster response. In principle, it performs the same voltage regulations function as the SVC but in a more robust manner because, unlike the SVC, its reactive current output capability is not impaired during severe busbar voltage depressions [37].

The following observations have been made with the EMTDC simulation of the MLVR-VSC operating as a STATCOM [24]:

- The MLVR-VSC can generate high pulse voltage waveform with very low THD (<2.5%) using the fundamental frequency for the main bridges and 12 times that frequency for the reinjection switches.
- The power switches in the main bridges can be connected in series without dynamic voltage balancing problems; the step-by-step increase and decrease

of output voltage reduces the *dV/dt* stress; the zero-voltage switching condition reduces the main bridge switching losses and the snubber requirement. These characteristics make the MLVR-VSC a suitable candidate for high power applications.

- Functioning as a STATCOM, the MLVR-VSC can provide full scale controllability of the capacitive and inductive power. With a full scale reactive power change the dynamic process can be completed in 40-60ms, and is therefore suited for compensation requiring fast response.
- As well as generating reactive power, the MLVR-VSC can supply some real power to a dc load with only a small fluctuation in the dc voltage. During active power exchange, the dc capacitor voltage of the MLVR-VSC can be balanced by appropriate adjustments of the reinjection switch on-state intervals.
- For asymmetrical source conditions, if the source voltage asymmetry is not very large, the MLVR-VSC can operate normally, and even inject more capacitive current to the lower voltage phase or absorb less inductive current from the lower voltage phase.
- Further study is needed to develop new control strategies to achieve symmetrical operation under asymmetrical source conditions.

2.5.2 HVdc Back-to-back

The HVdc-VSC comprises two VSCs, one operating as a rectifier and the other as an inverter, connected either back-to-back or joined together by a dc cable, depending on the application. Its main function is to transmit controllable dc power from the rectifier to the inverter station. One VSC controls the dc voltage and the other the transmission of active power through the dc link. During normal operation, it is desirable to have independent reactive power control of the two converters [4]. However, this is not possible for two converters, switched at fundamental frequency, connected in back-to-back fashion.

In reference 30, the following observations have been made from the EMTDC simulation of MLVR-VSC in HVdc back-to-back configuration:

- Under the fundamental switching frequency for the 12-pulse main bridge, the MLVR-VSC can generate a multi-level voltage waveform with about 5%

THD. The harmonic current penetration into the ac system can be controlled with a suitable value of the leakage reactance of the interface transformer.

- Although independent amplitude control at both ends is not available, the dual converter system can operate under normal and fault conditions (to some degree) to transfer active power bidirectionally between two separate ac systems and to inject or absorb reactive power at both sides. However, the reactive power injected into, or absorbed from, the two ac systems cannot be controlled independently.
- Based on the proposed control structure and strategy, the dual converter system can respond quickly to track the operating condition order with satisfactory dynamic and steady-state characteristics.

2.6 Fundamental Modulation Method to Achieve Flexibility in HVdc-VSCs

The modulation method controls the fundamental output by modifying the converter ac side harmonics relationship with the dc bus voltage. Mathematically, the parameter, which was otherwise constant, relating the dc bus voltage to the ac side fundamental component is made to be a variable. This variable parameter is widely named as the *modulation index*. Practically, the ac fundamental-dc voltage flexible relationship can be realised by introducing notches on an otherwise rigidly shaped waveform. The width, depth and location of these notches will depend on the control philosophy and level of modulation required. When the busbar is at normal conditions without severe voltage depresses, the required modulation level of a converter ac fundamental output in order to adjust its generated reactive power is within a limited range.

PWM is the most widely accepted modulation method for converters in low to medium power applications. It offers high flexibility ac output control at the expense of generating high order harmonics, which can be filtered by small inductors. However, PWM suffers greatly from high switching losses and large snubbers required to absorb the energy associated with high-power, high-frequency switchings. For these reasons PWM is not attractive for high power applications.

Modulation in MLVR-VSC is limited by the fact the 12-pulse main bridge has to maintain zero voltage commutations and the injected ac components on the dc side can only consist of in-phase components. Hardware minimisation by generating the

reinjection ac components, for both V_{YY} and $V_{Y\Delta}$, with one common circuit has further increased the limitations. Consequently, although modulation in MLVR-VSC is also performed via waveform notchings, the process is much more complicated and constrained than PWM based VSCs. Chapter 3 discusses the waveform shapes acquired by the dc voltages, in order to achieve modulation, and the corresponding harmonic effects on the ac side. Chapter 4 discusses the hardware topology and switching strategy adopted to achieve the waveforms discussed in chapter 3.

2.7 Conclusion

By adopting the harmonic cancellation concept, an ac/dc converter can output good quality ac waveforms without the assistance of PWM. Two symmetrical approximations of the ideal reinjection deduced in the harmonic cancellation concept to output zero THD ac waveforms are the ESEDS and linear symmetrical reinjection. The MLVR-VSC is a VSC based on the symmetrical reinjection concept with advance features such as soft-switching, low ac harmonic content and low dV/dt stress across the main bridge valves. These advance features are needed at high power, high voltage applications like STATCOMs and HVdc-VSCs. The MLVR-VSC can be brought a step further to embrace fundamental output control in order to enhance reactive power flexibility when applied for HVdc transmission systems. The fundamental output modulation via waveform notching method will be the research focus of this thesis.

Chapter 3

Harmonic Performance of the Modulated MLVR-VSC

3.1 Introduction

Output voltage control of an ac/dc converter is desirable for reactive power flexibility when two converters are linked together via a dc intertie. One of the possible methods to achieve this is by modulating the Fourier component magnitudes through notching the ac output waveforms. The PWM concept is the most accepted method for its ability to mitigate low order harmonics and voltage output controllability. Both CSC [42 & 44] and VSC [4, 21 & 33] can adopt PWM for low to medium power conversions. VSC's voltage notchings are usually performed at high frequency to meet the harmonic requirement of the power system while low frequency notchings have been reported for CSC control. The output waveform quality of the slower switched CSCs is improved by multiple converters connected to the power system with phase-shift transformers.

Due to the fact that modulation requires semiconductors with switch-off capability, self-commutated switches are employed for converter with modulation feature. Low to medium power PWM-VSCs are usually operated at high switching frequency and IGBTs employment are commonly reported [25]. Thyristor based GTOs, which are order of decades slower than the transistor based devices, have been used in proposal PWM-CSC [47].

MLVR-VSC is suited for high power, high voltage application with many features unavailable or difficult to achieve with the PWM based VSC. The ZVS of the main bridge commutations reduces snubber design complexity and switching losses significantly. By virtue of ZVS, the dynamic voltage sharing of semiconductors in a series chain is not an issue. Without modulation, fundamental switching frequency is maintained at the main bridge while good ac waveform quality is ensured by adopting the linear reinjection concept. Due to the low switching frequency and ZVS, technically any

self-commutated switches (GTOs, IGBTs and IGCTs) can be employed as the main bridge valves.

Ironically, however, the excellent harmonic performance of the MLVR-VSC has to be compromised in order to enhance the MLVR-VSC with modulation capability needed for reactive power flexibility in HVdc applications. In this thesis, trapezoidal, instead of the original triangular reinjection waveforms, have been utilised so that notches can be added to their flat tops and their gradients are adjusted according to the notch width. These notches have brought about the increase of low order harmonics, which require large filters, instead of high order ones as in the case of PWM-VSC. This harmonic impact caused by the modulation process, can be subdued further by increasing the reactance between the converter output voltage and the power system source.

This chapter discusses the modulation in MLVR-VSC strictly from the waveform point of view. Harmonic analysis for both ac voltage and current outputs based on ideal waveforms (infinite step number) are presented. The harmonic current penetration into the power system is investigated for a worse case scenario where the reactance between MLVR-VSC and the power system voltages is contributed only by the interface transformer leakage reactance.

The practical synthesized dc varying waveforms have to be quantised to some finite levels due to limitations on circuit complexity and size. The harmonic effects of finite quantisation levels are investigated for prudency. Hardware issues had lead to non-homogeneous step widths of the synthesized waveforms. This effect is also investigated in this chapter.

3.2 Fundamental modulation in VSC

3.2.1 Conventional Modulation Method for PWM Based VSC

Fundamental modulation in a VSC is generally performed via notching part of the converter ac voltage waveform. By having controllable notches widths, depths and locations on the waveform, the ac voltage Fourier components relationship with the dc side voltage can be modified.

The PWM concept is commonly used to achieve fundamental component control in a VSC. The notches in the PWM scheme can appear with widths and at time location as specified by the control and modulation philosophy used while the depths are usually limited by the hardware topology chosen to implement the VSC. Switching functions of the main bridge are modified accordingly to yield controlled amplitudes of fundamental and harmonic components. Figure 3.1 shows an example of the output voltage of a PWM-based 2-level VSC with sinewave-PWM technique (SPWM).

The common practice for PWM implementations in VSCs is to decrease the widths of the modulation notches and increase the notching frequency so that the harmonic content created by this modulation process will mainly appear at high frequency order. This has the effect of reducing cost and size of the ac filter required to filter these harmonics. Thus, PWM based VSCs usually use faster transistor based semiconductor devices to build its valves. However, these devices suffer from low reliability when series connected in order to withstand high dc bus voltage.

The PWM method suffers greatly from low efficiency and high dynamic voltage stress. Switching losses of the PWM-VSC are high due to hard-switching of the valves, i.e. valves are required to change states at rated current or voltage or both. The snubbers required to absorb the energy released by such switching events are very large and bulky. Soft-switching by using resonant type snubbers is not straight forward because the notched powers (time-current-voltage product) are not quite homogeneous over the fundamental period. Moreover, voltage across the valves ramps up from zero to rated voltage or ramps down from rated voltage to zero very quickly, inducing high dynamic voltage stress (dV/dt) on the semiconductor devices, interface transformer and cables. Hence, PWM-VSC is not suitable for transmission level applications, where tolerance to such problems is very rigid.

3.2.2 Fundamental Modulation in MLVR-VSC

A fundamental modulation method in MLVR-VSC has to avoid all the problems faced by the PWM-VSC for high voltage applications. Notches are introduced directly on the dc side voltage waveforms rather than modifying the main bridge switching functions. In this thesis, the linear reinjection concept, presented in section 2.3.3, has been adopted.

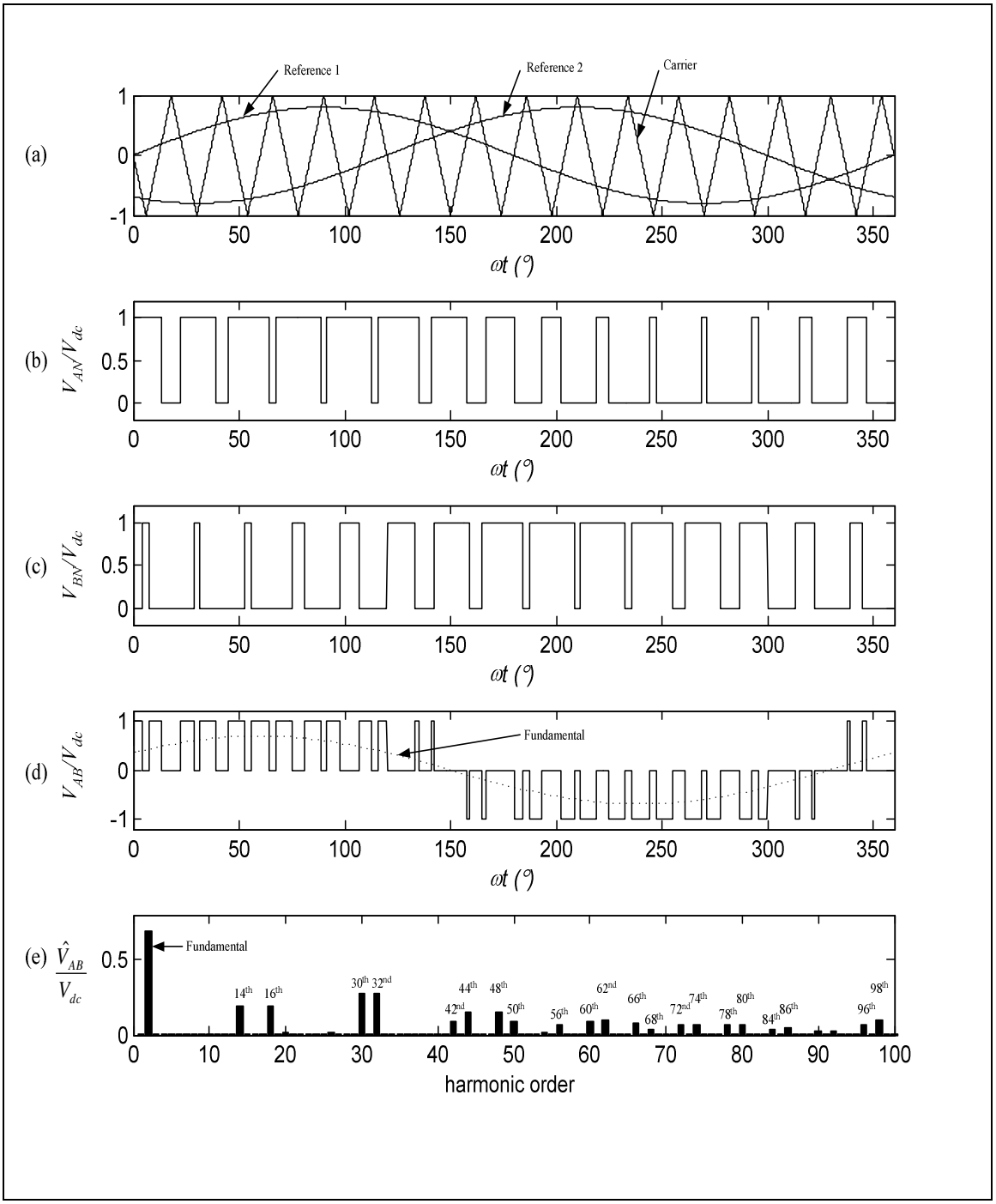


Figure 3.1 Two-level SPWM method for the conventional 6-pulse VSC. [1]
(a) Reference signals and carrier signal (triangular) (f_c=15f_1);
(b) Voltage Waveform V_{AN};
(c) Voltage Waveform V_{BN};
(d) Line-to-line output voltage waveform V_{AB}; and
(e) Normalised harmonic amplitude of the voltage waveform V_{AB}.

The triangular reinjection voltage waveforms are modified into trapezoidal shapes with their flat tops being notched consistently every 60° period .

3.2.2.1 Waveform Restriction of MLVR-VSC

The harmonic cancellation concept functions on the basis that specified harmonics are injected on the dc side of the 12-pulse converter in order to cancel harmonics of order $n=6(2l-1)\pm1$ ($l=1,2,3\ldots$) on the ac side waveforms. The infinite series in equation 2.3.2.1 and 2.3.2.2 bound these harmonics to be $6k^{th}$ ($k=1,2,3\ldots$) order of the fundamental frequency and their corresponding amplitudes to be the solution for equations 2.3.2.5 and 2.3.2.6. This implies that the dc voltage waveforms appearing to the main bridges to be varying at 6 times the fundamental frequency and they are identical over every 60° period.

Only cosine (in-phase with fundamental) components are injected on the converter dc side as prescribed by the harmonic cancellation concept. Sine (out-of-phase with fundamental) components are avoided because they induce second order ac side harmonics which cannot be cancelled by the 12-pulse bridge operation. This exclusion further imposes the limitation on the main bridge dc voltage waveforms to have even symmetry about the vertical axis of 30° (half of the 60° period).

The relationship between both main bridges reinjection harmonics has to fulfil the condition mentioned in last paragraph of section 2.3.2 where the reinjection harmonic amplitudes, A_{Yk} and $A_{\Delta k}$, must be equal for all values of k. The displacement between the $12k^{th}$ reinjection harmonics of both bridges have to be in-phase while the $6(2k-1)^{th}$ reinjection harmonics have to be half period phase-shifted. Graphically, this condition is translated to 30° (of fundamental period) phase-shift between V_{YY} and $V_{Y\Delta}$.

3.2.2.2 Restriction Caused by Complementary Main Bridges

Provided that the waveform restrictions of section 3.2.2.1 are obeyed, notches can be added mathematically anywhere along a 30° section of the dc side voltage waveforms in order to achieve fundamental modulation while upholding the harmonic cancellation concept. The solutions of equations 2.3.2.5 and 2.3.2.6 yield V_{YY} and $V_{Y\Delta}$ that are not

symmetrical about their dc average axis, hence when V_{YY} and $V_{Y\Delta}$, which are phase-difference by 30°, are added together, they will yield a dc average with some ripples.

Symmetrical approximations to equations 2.3.2.5 and 2.3.2.6 have to be made so that V_{YY} and $V_{Y\Delta}$ will be complementary of each other. Complementary waveforms will reduce the circuit cost and complexity, in exchange for slightly increased harmonic content on the ac side.

Two approximations can be made to approximate the V_{YY} and $V_{Y\Delta}$ to be complimentary and yield $V_{YY}(\omega t) + V_{Y\Delta}(\omega t) = V_{dc}$, where V_{dc} denotes the MLVR-VSC dc bus voltage. One approximation yields waveforms with linear characteristics (linear reinjection) while the other yields non-linear waveforms. The non-linear waveforms (ESEDS reinjection) will reflect ac voltage waveforms with slightly lesser harmonic content than the linear reinjection. However, the ac voltage harmonic content difference between them becomes insignificant when the waveform level number, m, becomes greater than 8. Additionally, the linear reinjection synthesis circuit, where the dc varying waveform shape is 6 identical triangles over a fundamental period, is far more economical than that for the non-linear ESEDS reinjection.

The complimentary relationship between V_{YY} and $V_{Y\Delta}$ implies that notching on one waveform will cause bulging of the other. If these bulges are allowed to be reflected onto the ac side, they will annihilate the notches when two primary winding voltages, of Y/Y and Y/Δ transformers, are summed together on the ac side. The only way to eliminate this problem is to modify the 12-pulse converter bridge valves switching patterns.

High converter efficiency is required for very high power application. The main bridge valves commutate at zero voltage to reduce switching losses in the MLVR-VSC. Therefore, zero voltage level has to be synthesised prior and after the bulges so that switch states of the 12-pulse valves can be modified in order to disregard the complementary bulges. For example, if the V_{YY} waveform is notched at some time, a complementarily synthesized bulge will be seen across the Y/Δ main bridge. This bulge is undesirable and the Y/Δ main bridge valves switch states are changed just moments prior so that the complimentary bulge will not be reflected onto the interface transformers. At a time after the notch has been removed, the Y/Δ main bridge switch states are restored to those prior to notching. Chapter 4 discusses the MLVR-VSC switching patterns in detail.

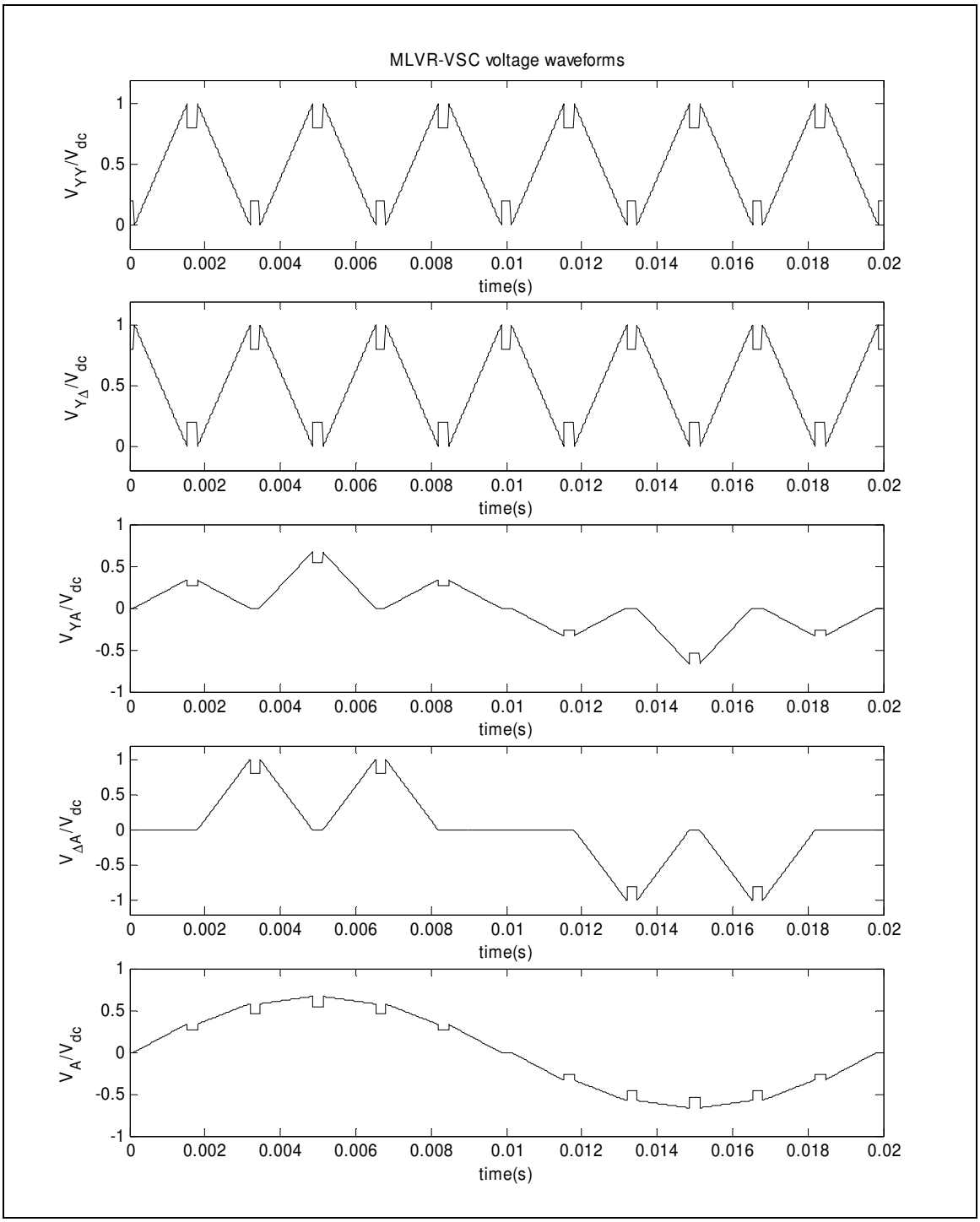


Figure 3.2 Voltage waveforms for the modulated ideal linear MLVR-VSC.

Legend

V_{YY} : varying dc voltage waveform applied to Y/Y connected 6-pulse converter
$V_{Y\Delta}$: varying dc voltage waveform applied to Y/Δ connected 6-pulse converter
V_{YA} : phase A output voltage of Y/Y connected 6-pulse converter
$V_{\Delta A}$: phase A output voltage of Y/Δ connected 6-pulse converter
V_A : total phase A output voltage of MLVR-VSC

Under the ZVS objective, the switch states of the main bridge valves can be changed only when zero voltage appear across the main bridge. Therefore, the complimentary bulges can only occur at times when the V_{YY} or $V_{Y\Delta}$ is zero before and after its occurrence. This limits the locations of these complementary bulges to be around 0°, 60°, 120°, 180° etc. for V_{YY} and around 30°, 90°, 150°, 210° etc. for $V_{Y\Delta}$. The specified locations of complementary bulges requires that the notches on V_{YY} can only occur at times around 30°, 90°, 150°, 210° etc. and the notches on $V_{Y\Delta}$ can only occur at times around 0°, 60°, 120°, 180° etc. These restrictions, together with the objective of fundamental modulation, have resulted in the varying dc waveforms with notched top trapezoidal shape. Figure 3.2 shows an example of the voltage waveforms of the modulated MLVR-VSC with ideal (infinite step level number) linear reinjection. Notice how notching on V_{YY} will cause bulging on $V_{Y\Delta}$ and vice versa and that these notches do not appear on the bridges ac output voltage. The total per phase output voltage resembles a sine waveform with 12 regularly occurring rectangular notches.

3.3 MLVR-VSC Harmonic Analysis

3.3.1 Voltage Harmonics

Due to harmonic cancellation and three phase symmetry reasons, all the 12 notches on the varying dc waveform have to be similar. Hence, for specific transformer transformation ratio and dc bus voltage, the output voltage Fourier analysis is solely dependent on the width, W, and the depth, d, of these notches. Figure 3.3, shows the expanded view of modulated V_{YY} waveform with the notch width (W) and depth (d) clearly shown. Again, the complementary bulges only appear on the dc side and are not reflected onto the ac output.

The MLVR-VSC in this thesis is investigated for balanced operation only. Hence, output voltage waveforms analysed for one phase are essentially identical to the other two. Here, harmonics analysis is performed on phase A. The Fourier components of the ideal linear MLVR-VSC phase A voltage is written as

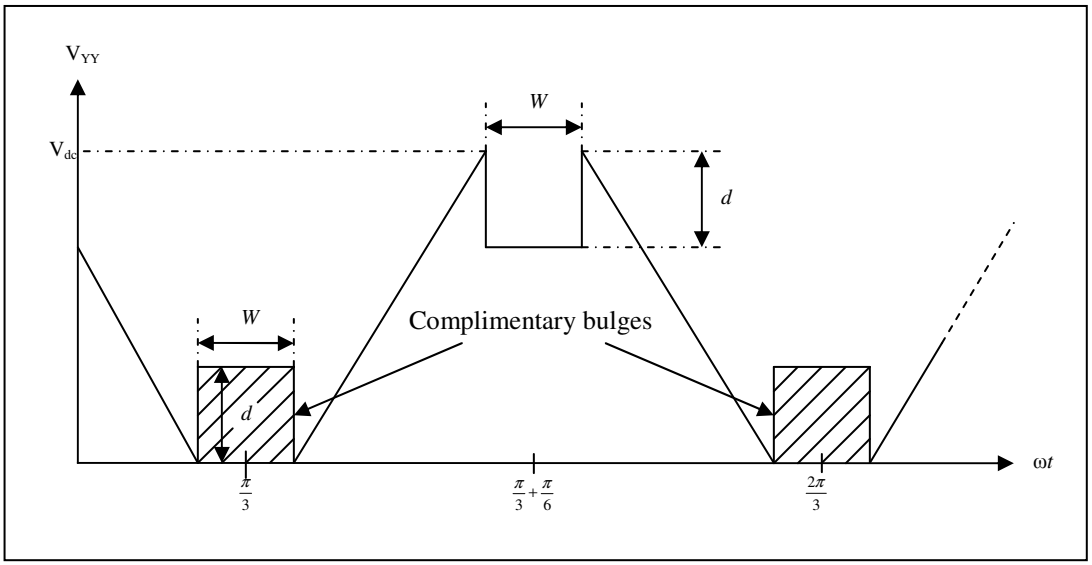


Figure 3.3 Expanded view of ideal linear modulated V_{YY} waveform.

$$V_{An} = \frac{8V_{dc}a}{3n\pi}\left\{\frac{2\sin n\left(\frac{\pi}{12}-\frac{W}{2}\right)\cos\frac{n\pi}{6}\cos\frac{n\pi}{12}}{n^2\left(\frac{\pi}{6}-W\right)}\left[4\sqrt{3}-7-4\left(\sqrt{3}-2\right)\cos^2\frac{n\pi}{12}\right]-f_{Vn}(d,W)\right\} \tag{3.3.1.1}$$

Where

$$f_{Vn}(d,W) = \frac{d}{100}\sin\frac{nW}{2}\sin\frac{n\pi}{3}\left(2\cos\frac{n\pi}{6}+\sqrt{3}\right) \tag{3.3.1.2}$$

a = transformation ratio of interface transformer

V_{dc} = dc bus voltage

$n = 1,12k \pm 1$ *for* $k = 1,2,3...$

From equation 3.3.1.1, the fundamental component is

$$V_{A1} = V_{dc}a\left[\frac{8\sqrt{2-\sqrt{3}}}{\pi(\pi/6-W)}\sin\left(\frac{\pi}{12}-\frac{W}{2}\right)-\frac{2d}{25\pi}\sin\frac{W}{2}\right] \tag{3.3.1.3}$$

When the dc bus voltage, V_{dc}, is fixed the parameters d and W are controlled to vary the fundamental component amplitude in equation 3.3.1.3. It is obvious that the larger the area being notched away from the waveforms, the smaller will be the fundamental component amplitude reflected on the ac side. There are many solutions to equation 3.3.1.3 for some value of V_{A1}. However, the parameter d is practically limited by hardware issues such as topology step number and high dV/dt induced on the valves. Therefore, d is usually kept at some constant level for specified level number topology while W is varied to achieve the fundamental modulation level required.

The range of fundamental amplitude control to achieve 100% reactive power flexibility is dependent on the interface transformer leakage reactance. A 0.1 p.u. interface leakage reactance will infer a 10% fundamental modulation level (refer chapter 1 for mathematical verification). From equation 3.3.1.3, the maximum value for V_{A1} is $0.65aU_{dc}$ when both d and W are zero. Assuming this is the line-to-ground rated voltage (amplitude) of the MLVR-VSC, 10% fundamental modulation will result in V_{A1}=$0.59aU_{dc}$.

The plots in figure 3.4 show the normalised V_{A1} against V_{dc}, i.e. assuming unity transformation ratio, for various values of d and W. Ten plots are drawn for specified d from 0% to 100% while W is varied from 0° to 25°. For this range of W, equation 3.3.1.3 is almost a linear function to W. The dashed line marked the 10% modulation level. It can be seen that when d is smaller, the modulation effect by varying W is less. Therefore, the setting of d has to be performed taking account that while wider W is required for higher modulation level its range is also limited. Mathematically, W can be in the range of 0° to 30° but the practical limit is lesser. Wide W will cause the V_{YY}, in figure 3.3, and $V_{Y\Delta}$ waveforms to have steep rising and falling slopes. A steep gradient implies that faster synthesis circuit is needed and the dV/dt stress on the main bridges is higher.

The waveform quality impact of notching is analysed by investigating the total harmonic distortion (THD) and the individual harmonic components on the ac output. The rms value of V_A as a function of d and W is

$$V_{Arms} = V_{dc} a \sqrt{\frac{2}{9\pi}\left\{\frac{\left(4+\sqrt{3}\right)\pi}{6} + W\left[6\left(1-\frac{d}{100}\right)^2 - 4 - \sqrt{3}\right]\right\}} \qquad (3.3.1.4)$$

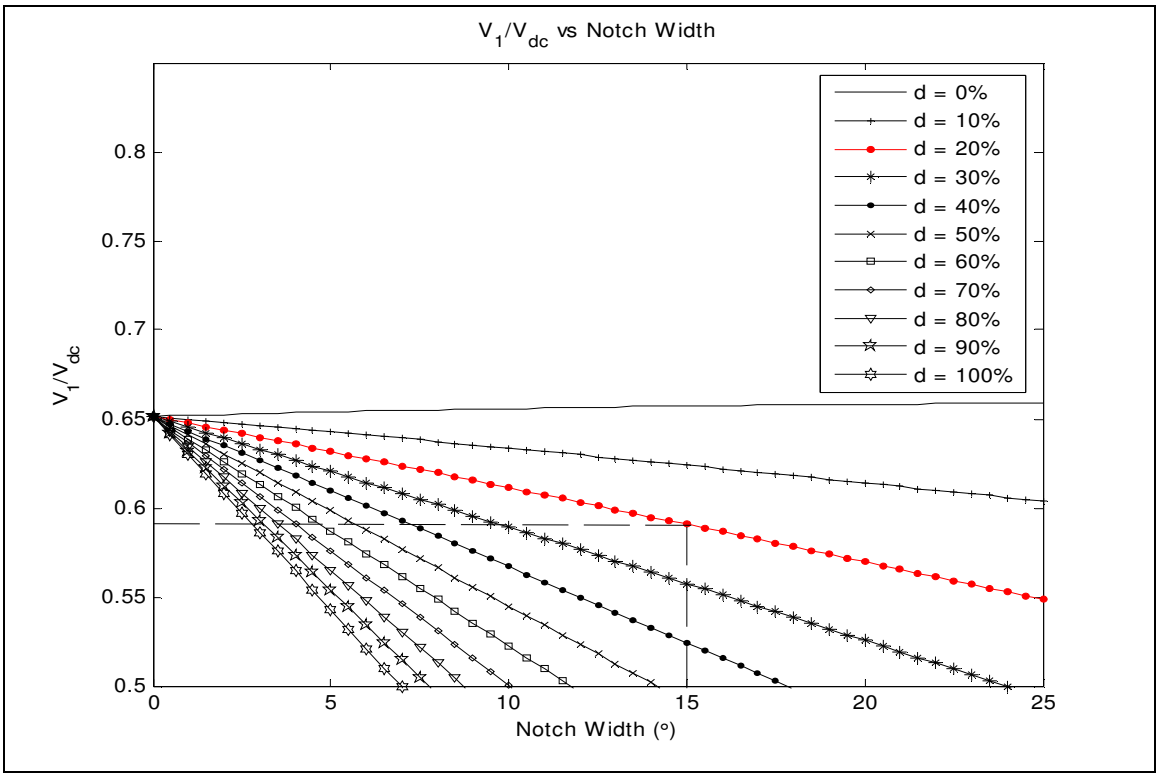


Figure 3.4 Normalised MLVR-VSC output voltage fundamental component against *W*.

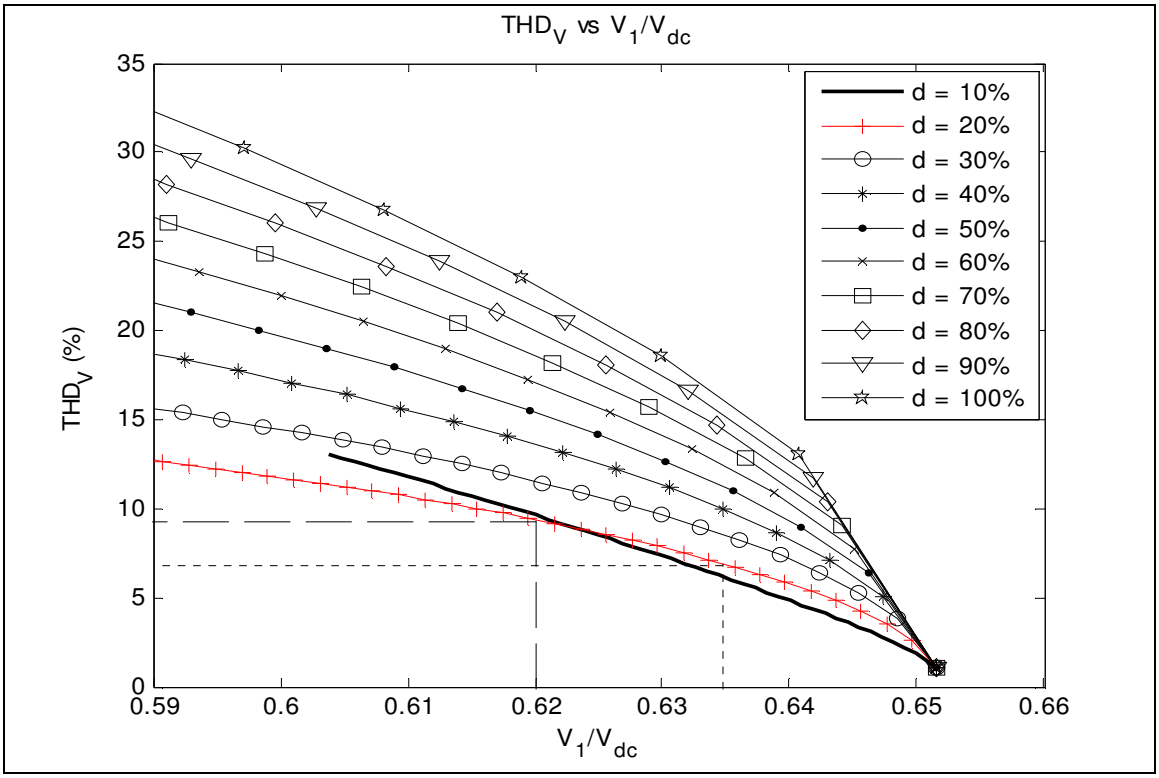


Figure 3.5 MLVR-VSC output voltage THD against normalised fundamental component.

and the MLVR-VSC ac output voltage THD is

$$THD_V = \left(\sqrt{\frac{2V_{Arms}^{\ 2}}{V_{A1}^{\ 2}} - 1} \right) \times 100\% \qquad (3.3.1.5)$$

The general behaviour for THD_V is that the harmonic content for shallower d and wider W will be lower than deeper d and narrower W. While this can be used as a guideline in specifying the d parameter during notching, the practical constraints mentioned before also have to be considered. Figure 3.5 plots the THD_V against the normalised fundamental component for 10 values of d. Note that limited plot step has caused some plots in figure 3.5 to appear as linear in the range for $0.64<V_1/V_{dc}<0.651$ although they should follow the general curves patterns as in other values. Also, the plots for d=10% is shorter than the rest because W has saturated to a maximum value and the minimum achievable V_1 is $0.604V_{dc}$. The detailed mathematical functions and integration operations to obtain equations 3.3.1.1-3.3.1.4 are listed in appendix C.

Unlike the PWM method, the 12 identical notches occurring at regular 60° on the MLVR-VSC dc side cause low order harmonics on the ac side. This is an indication that filters (if required) for MLVR-VSC connection to rigid power system may be large. The dominant low order harmonic (11^{th} to 49^{th}) components on the MLVR-VSC ac output are plotted in figure 3.6 based on equation 3.3.1.1. Appendix D provides harmonic component plots for up to the 97^{th} order.

3.3.2 Current Harmonics

For high power applications, the converters are usually connected to a strong power system, which can be approximated to an infinite bus with an ideal three phase voltage source. In such cases, the source internal impedance is negligibly small compared to the interface transformer leakage reactance, X_l. Also, for analytical purpose, the forward voltage drop of the switches can be ignored and the converter dc capacitance is assumed to be infinite. The interface transformer is assumed to be perfectly balanced and losses are ignored (both copper and iron). Under all these assumptions, the MLVR-VSC connected to a strong ac system can be modelled by the simplification shown in figure 3.7. The strong ac system is modelled as ideal voltage sources (V_{SA}, V_{SB} and V_{SC}) seen

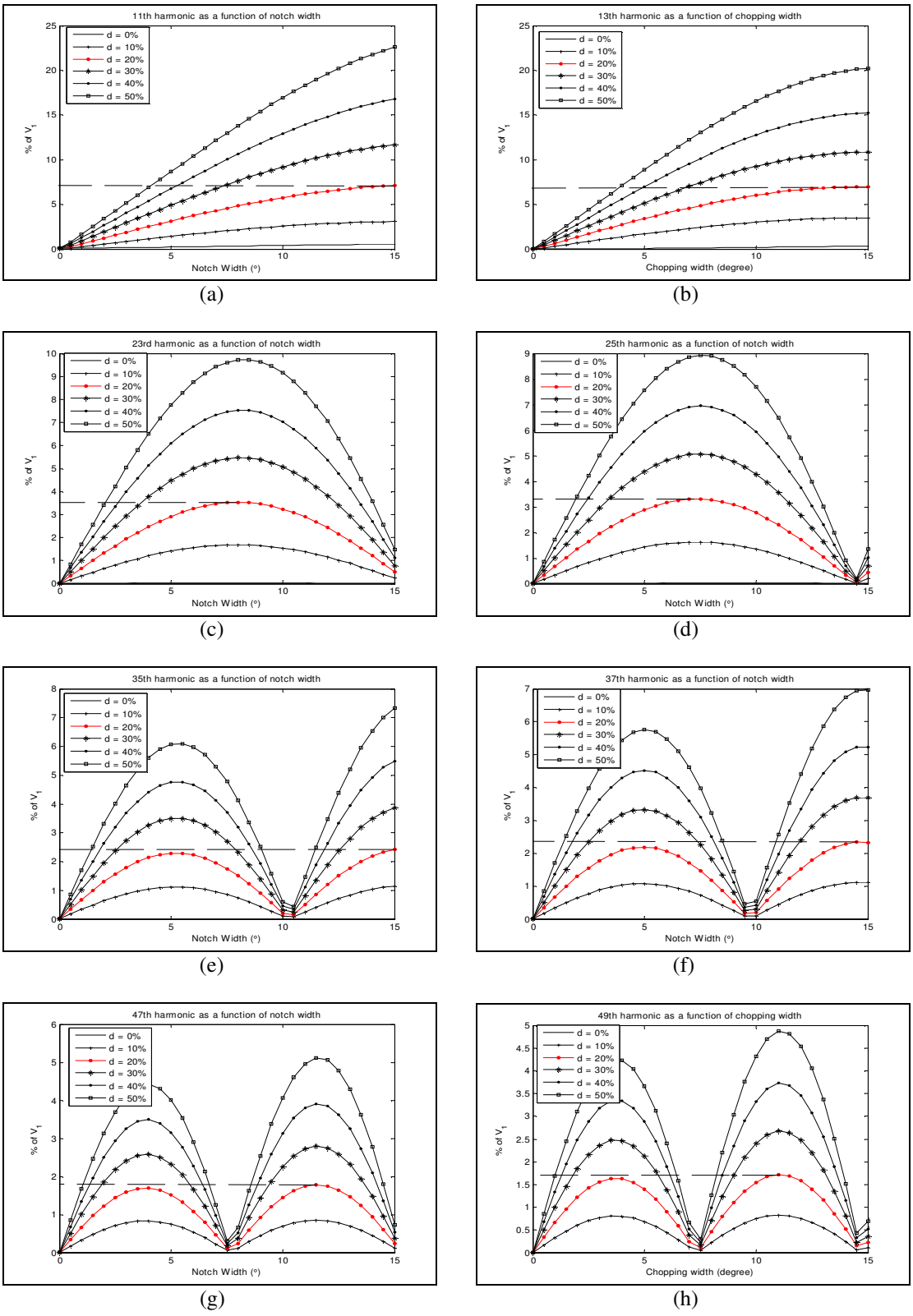


Figure 3.6 MLVR-VSC output voltage harmonic components

across the primary windings of the interface transformer. The converter is reduced to a three phase voltage source (V_A, V_B and V_C) with harmonics but without internal impedance. These two voltage sources are linked together via the interface transformer leakage reactance, X_l.

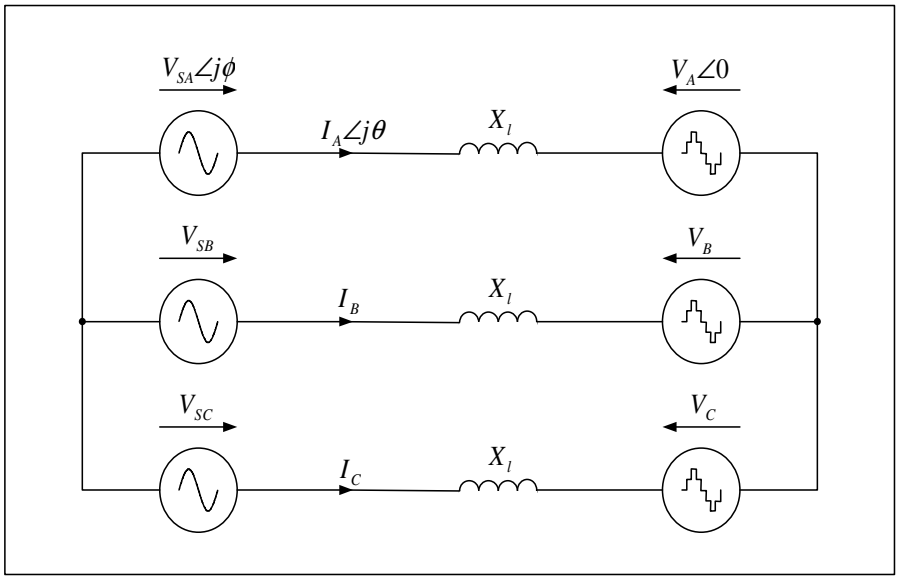


Figure 3.7 The simplified model of the MLVR-VSC connected to infinite bus.

For the simplified model in figure 3.7, the converter phase A output current, I_A, is governed by differential equations

$$L_l \frac{dI_A(\omega t)}{dt} = V_{SA}(\omega t) - V_A(\omega t) \qquad (3.3.2.1)$$

or

$$I_A(\omega t) = \frac{1}{X_l}\int_0^{\omega t} V_{SA}(\omega t)d\omega t - \frac{1}{X_l}\int_0^{\omega t} V_A(\omega t)d\omega t + I_A(0) \qquad (3.3.2.2)$$

where L_l is the leakage inductance of the transformer, X_l is the rated leakage reactance at fundamental frequency,

$$V_{SA}(\omega t) = \left[V_{Sm}\sin(\omega t + \phi)\right] \qquad (3.3.2.3),$$

and

$$V_A(\omega t) = \left[\sum_{n=1}^{\infty} V_{An} \sin(n\omega t)\right] \quad (3.3.2.4)$$

Since I_A is periodic over one fundamental period, $I_A(0)$ can be determined from the steady-state boundary condition, where $I_A(\omega t)|_{\omega t=0\rightarrow\pi} = -I_A(\omega t)|_{\omega t=\pi\rightarrow 2\pi}$. Hence, $I_A(0)$ becomes

$$I_A(0) = \frac{-V_{Sm}}{X_l}[\cos(\phi)] + \frac{1}{2X_l}\int_0^{\pi} V_A(\omega t)d\omega t \quad (3.3.2.5)$$

Substituting equation 3.3.2.5 into equation 3.3.2.2, $I_A(\omega t)$ in expanded form becomes

$$I_A(\omega t) = \frac{1}{X_l}\int_0^{\omega t} V_{SA}(\omega t)d\omega t - \frac{V_{Sm}}{X_l}[\cos(\phi)] - \frac{1}{X_l}\int_0^{\omega t} V_A(\omega t)d\omega t + \frac{1}{2X_l}\int_0^{\pi} V_A(\omega t)d\omega t \quad (3.3.2.6)$$

Since V_S is assumed to be ideal, the harmonic content of I_A is solely caused by the last two terms in the right had side of equation 3.3.2.6. Hence, performing time-integration of these terms will yield the harmonics amplitude of I_A. The output current harmonic amplitudes are related to the MLVR-VSC voltage harmonic amplitudes as

$$I_{An} = \frac{V_{An}}{nX_l} \quad (3.3.2.7)$$

The output current rms value and THD (THD_I) obtained by performing the integration of equation 3.3.2.6 are

$$I_{Arms} = \frac{V_{A1}}{\sqrt{2}X_l}\sqrt{k^2 + P(d,W) - 1} \quad (3.3.2.8)$$

and

$$THD_I = \left(\frac{\sqrt{P(d,w)-1}}{k}\right) \times 100\% \quad (3.3.2.9)$$

where $k=\sqrt{1+\frac{V_{sm}^2}{V_{A1}^2}-2\frac{V_{sm}}{V_{A1}}\cos\phi}$; (3.3.2.10)

$$P(d,W)=\frac{4f_I(d,W)}{\pi\left[\frac{8\sqrt{2-\sqrt{3}}}{\pi(\pi/6-W)}\sin\left(\frac{\pi}{12}-\frac{W}{2}\right)-\frac{2d}{25\pi}\sin\frac{W}{2}\right]^2} \quad (3.3.2.11)$$

and

$$f_I(d,W)=\left(\frac{\pi}{6}-W\right)^3\left(\frac{636+357\sqrt{3}}{540}\right)+W\left(\frac{\pi}{6}-W\right)^2\left[\frac{65+36\sqrt{3}}{18}-\frac{d}{100}\left(\frac{22+12\sqrt{3}}{9}\right)\right]$$
$$+W^2\left(\frac{\pi}{6}-W\right)\left(1-\frac{d}{100}\right)\left[\frac{11+6\sqrt{3}}{3}-\frac{d}{100}\left(\frac{4+2\sqrt{3}}{3}\right)\right]+W^3\left(1-\frac{d}{100}\right)^2\left(\frac{11+6\sqrt{3}}{9}\right) \quad (3.3.2.12)$$

From equation 3.3.2.9, it can be seen that the output current THD is dependent on the operation index, k, which describes the operating power of the converter. For a specific output voltage waveform, V_A, THD_I will vary between the lower limit, when k is equal to the per unit value of X_l, and infinity, when k is zero for zero apparent power. Figure 3.8 shows the MLVR-VSC phase A output currents of various k values for x_l=0.1p.u., d=20% and W=15°. Appendix C lists the complete steps to obtain equations 3.3.2.9-3.3.2.12.

In order for the waveform quality assessment to be meaningful, all the THD_I are plotted under the rated operation condition, i.e. $k=x_l$. Figure 3.9 and 3.10 show the output current THDs against normalised V_1 for x_l=0.1 p.u. and 0.05 p.u. respectively. The corresponding dominant low order harmonics (11^{th} to 49^{th}) are plotted in figure 3.11 and 3.12. Appendix D provides current harmonic plots up to the 97^{th} order.

The output current harmonic content follows the characteristics of voltage harmonic content: for the same level of modulation, deeper d and narrower W will lead to more THD_I compared to shallower d and wider W. The merit of THD_I is generally lower than THD_V is caused by the filtering effect of X_l. For practical applications, the p.u. value of X_l is between 0.03 to 0.1. Although smaller X_l requires less fundamental voltage modulation range to achieve more reactive power control, and hence lower voltage THD,

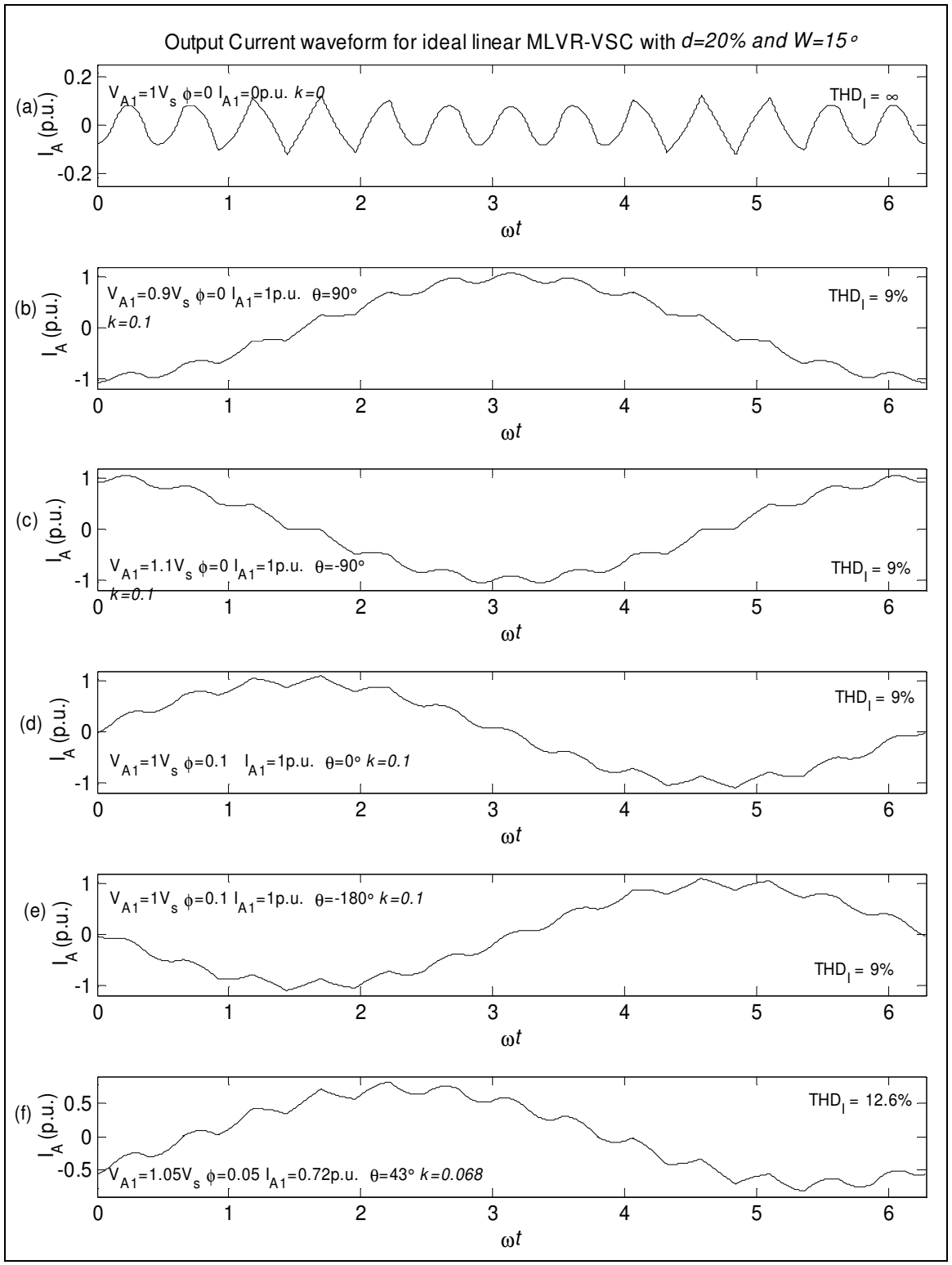


Figure 3.8 The output current waveforms of ideal linear MLVR-VSC with d=20%; W=15° and x_l =0.1p.u.

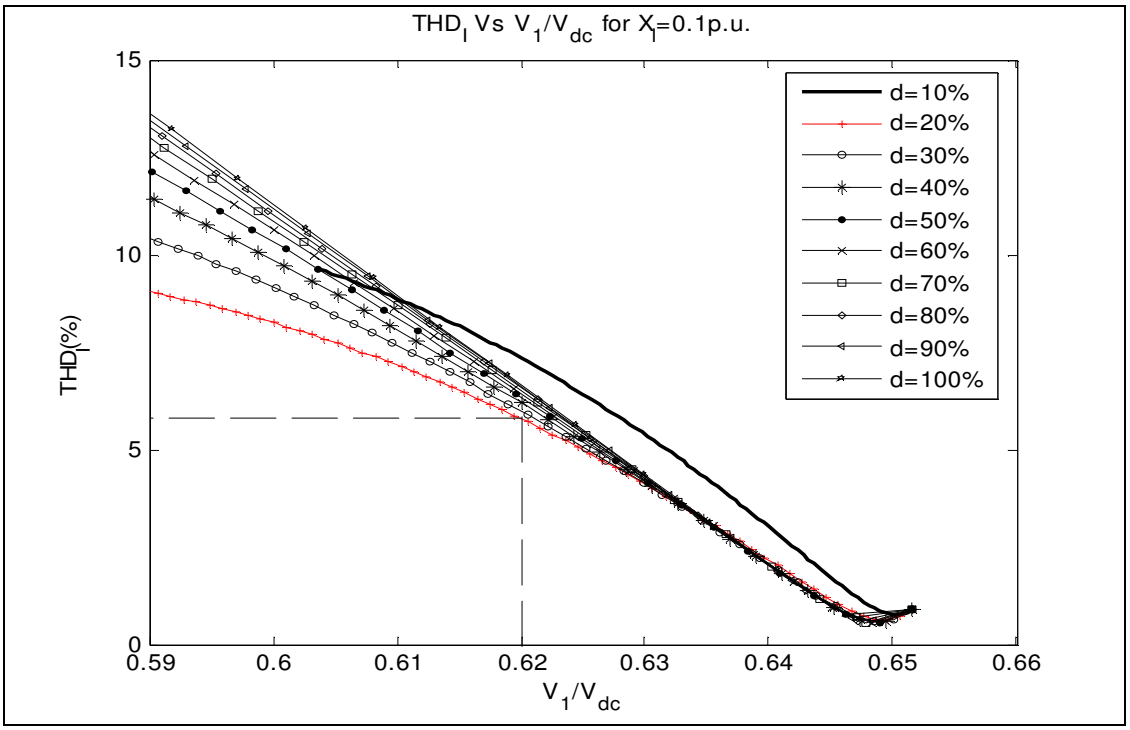


Figure 3.9 MLVR-VSC current THD against normalised fundamental component for x_l=0.1p.u.

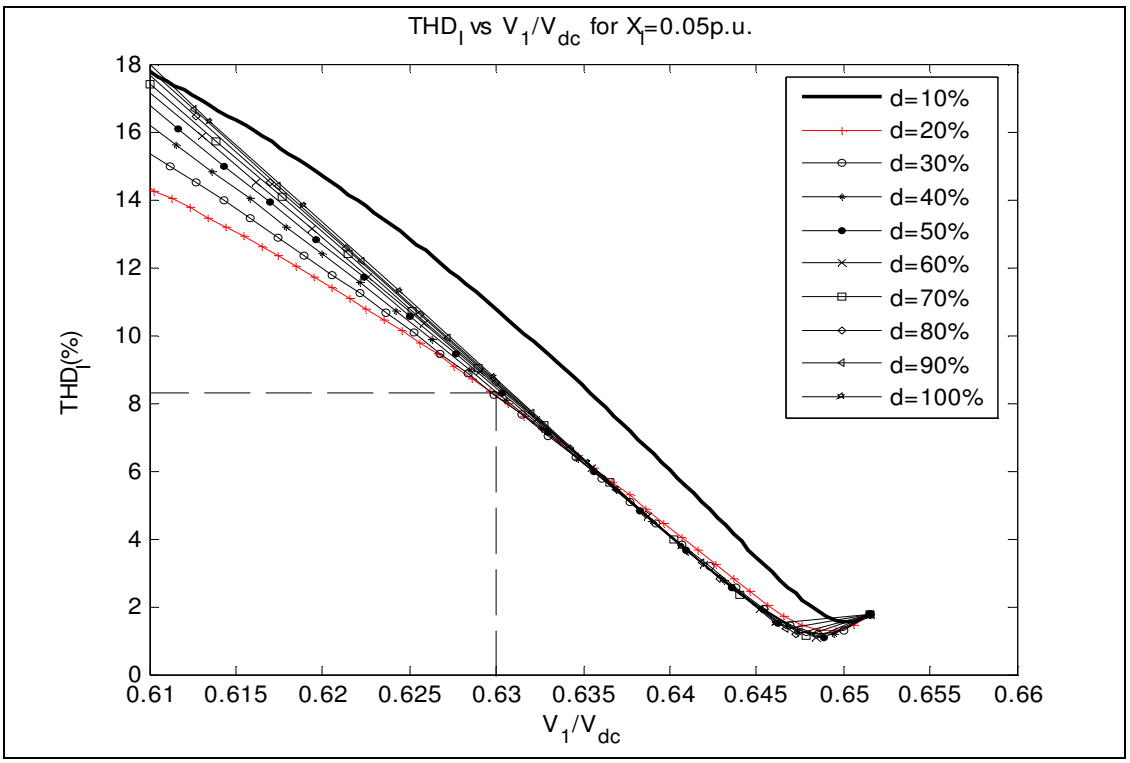
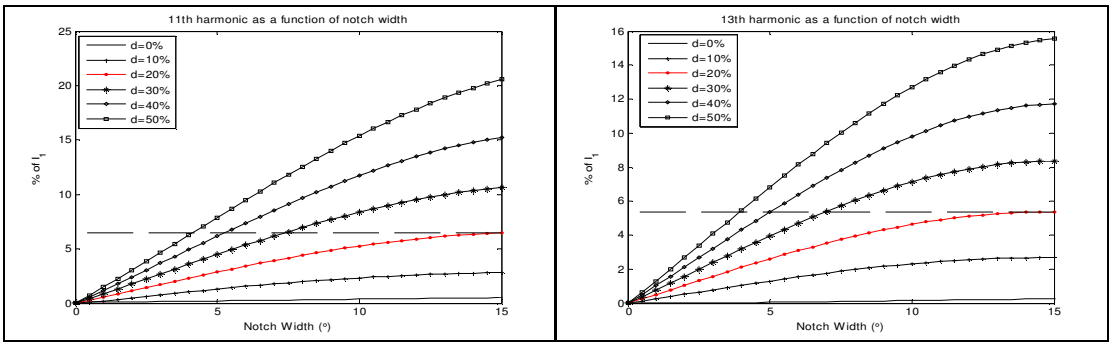


Figure 3.10 MLVR-VSC current THD against normalised fundamental component for x_l=0.05 p.u.



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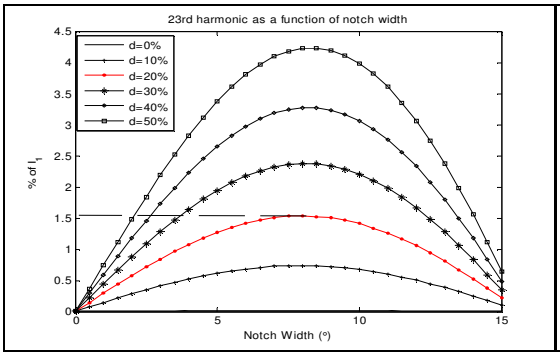
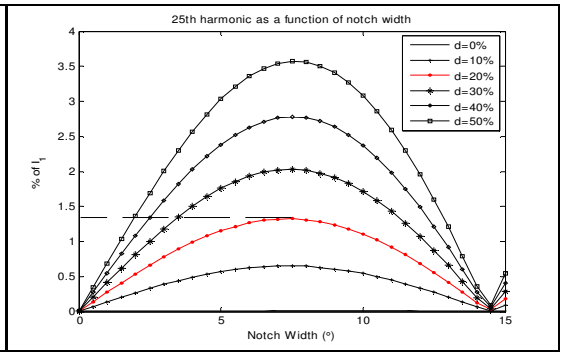


(c)



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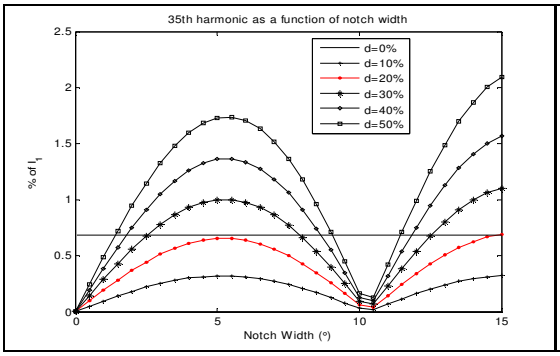

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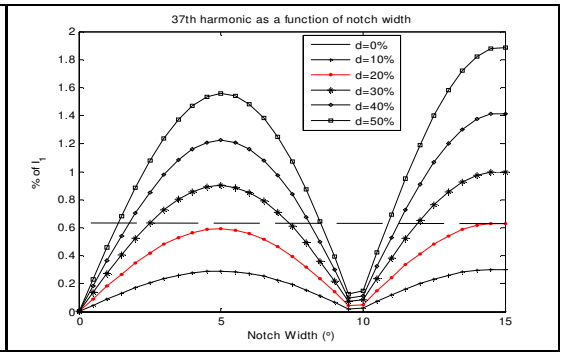

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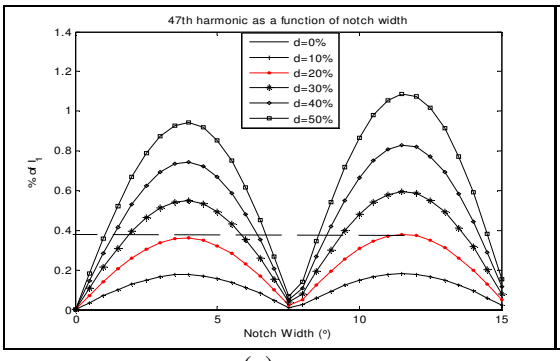

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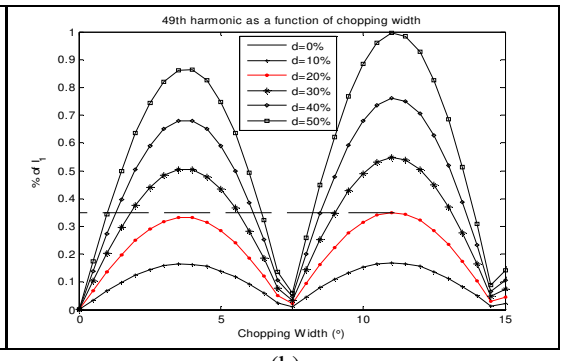
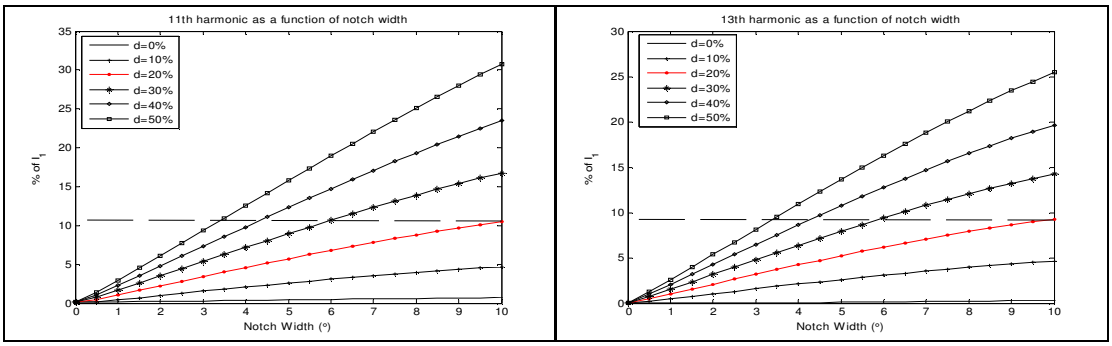


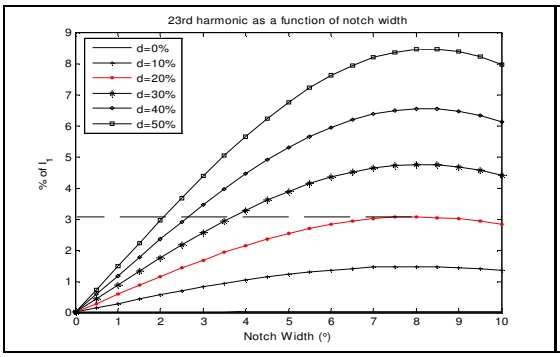
(h)

Figure 3.11 MLVR-VSC current harmonic components for 0.1 p.u. x_l.



(a)

(b)



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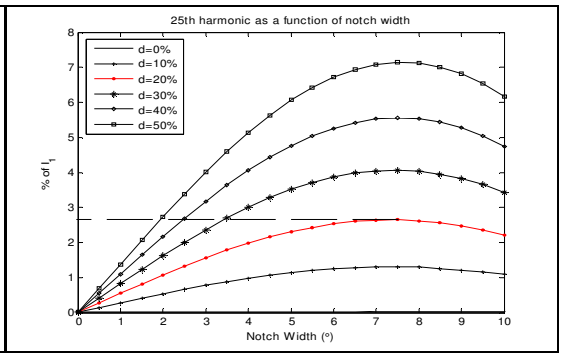

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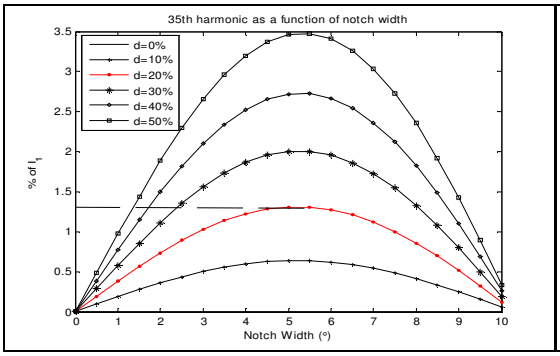

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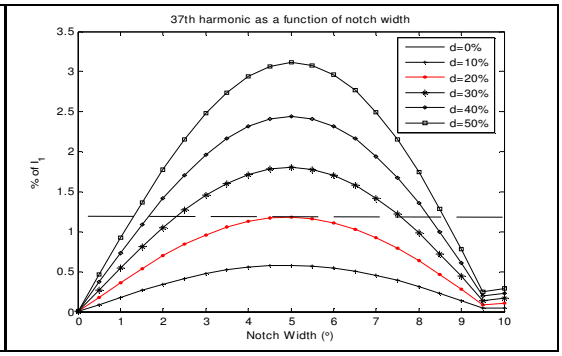

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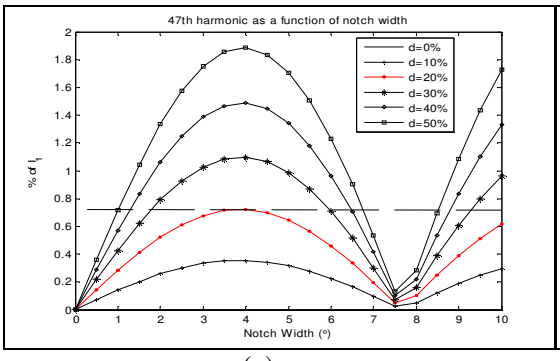

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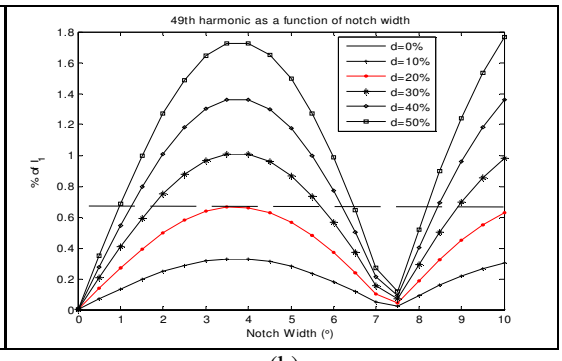


(h)

Figure 3.12 MLVR-VSC current harmonic components for 0.05 p.u. X_l.

this is not the case for current. For x_l=0.1p.u., the THD_I for full modulation lies between 8%-14% while the full modulation THD_I for x_l=0.05p.u. lies between 14%-18%.

The interface transformer leakage reactance acts like a harmonic filter to the current. The corresponding voltage harmonic decrease due to lesser modulation level can not compensate for the decrease in filtering effect of the leakage reactance, i.e. V_n decrease rate is slower than that of nx_l. In the case of x_l=0.1 p.u., the attenuation effect of the leakage reactance at 11^{th} harmonic is almost none because nx_l=1.1≈1. Hence, figure 3.11(a) is similar to figure 3.6(a). In the case of x_l=0.05 p.u., the leakage reactance actually boosts the harmonics for up to n=20, i.e. nx_l<1 for n<20.

3.4 Non-ideal Voltage Waveforms

Equations 3.3.1.1-3.3.1.5 describes the MLVR-VSC with ideal linear waveforms (i.e. infinite step numbers). However, the synthesised voltage waveforms in practical implementations will consists of a finite step number. Additionally, the quantisation width, which should be equal for the linear reinjection concept, occasionally has to be varied for voltage sharing between capacitors. Chapter 4 discusses the purpose and mechanism of this voltage sharing in detail. Hence, it is also useful to investigate the effect of variation of the highest and lowest step width.

3.4.1 Finite Stepped Waveforms

Practically, the VSC waveforms will be quantified to discrete levels. For linear MLVR-VSC, each step level on the varying dc waveforms, V_{YY} and $V_{Y\Delta}$, is $V_l=V_{dc}/(m\text{-}1)$. If m is high enough, the harmonic characteristics of the MLVR-VSC will be identical to those of the idealised waveforms in section 3.3. An MLVR-VSC with m-stepped dc varying waveforms will output a $12(m\text{-}1)$-pulse ac waveform. The corresponding decrease in THD_V caused by increasing m on the dc side becomes insignificant when m>8. Therefore the discussions in this section are limited to m<12 quantisation level. However, there are advantages on hardware issues with high value of m: dV/dt stress on the main bridge switches is reduced by having smaller V_l, i.e. higher m, and the cost of redundancy for reliability purposes is also smaller by decreasing the voltage ratings of the dc sources used for synthesizing each quantisation level.

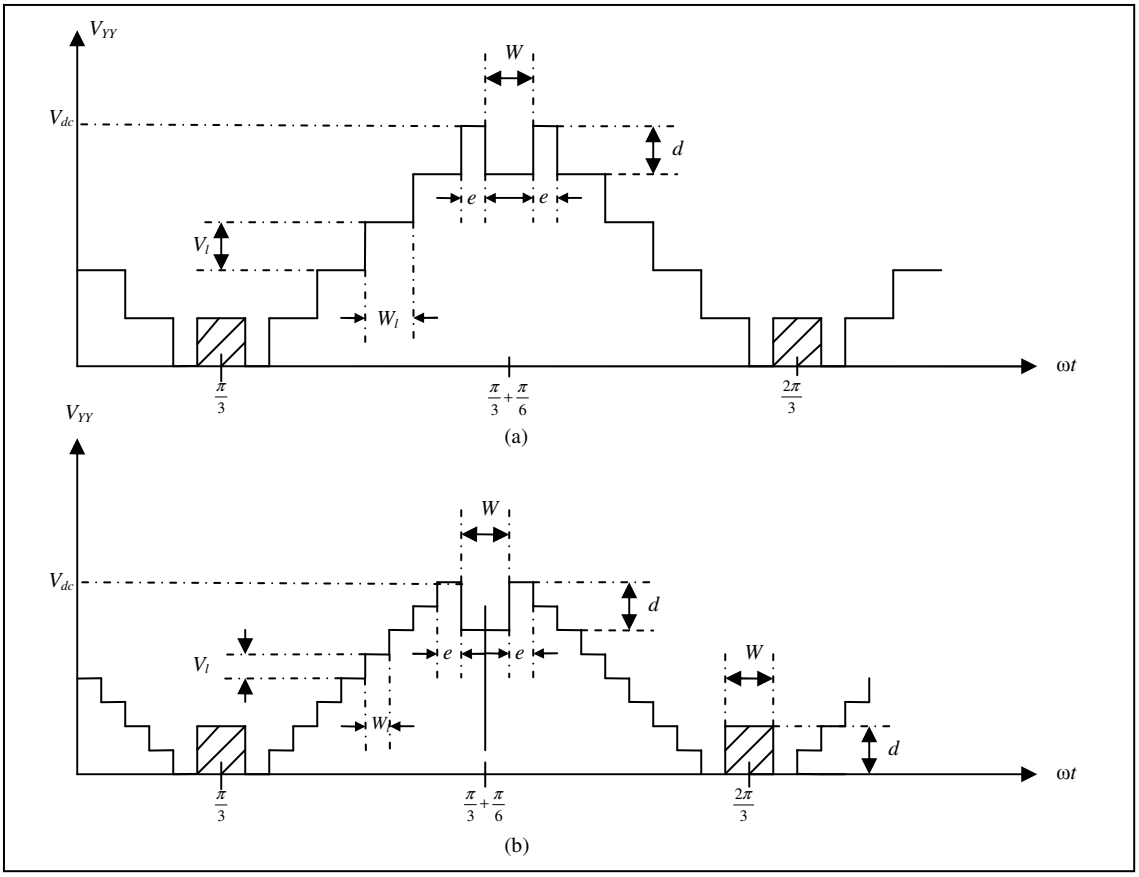


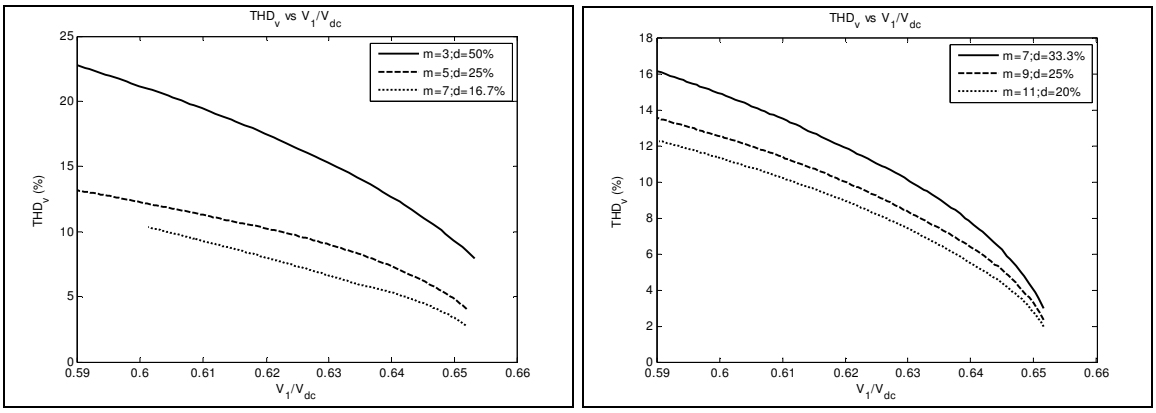
Figure 3.13 Expanded view of stepped-linear modulated V_{YY}.
(a) 5 step level
(b) 9 step level

Figure 3.13 shows the expanded view of stepped V_{YY} for m=5 and m=9. From the ideal analysis in section 3.3.1, lowest THD_V with full modulation is observed when d is at 20%. However, the explicit value of d will depend on m as d can only follow the integer multiple of V_l. For instance, when m<7, d is equal to 1 step level; for $7 \leq m \leq 11$, d is equal to 2 step levels etc. Table 3.1 lists the levels of d for some values of m.

Figure 3.14 shows the THD_V against the normalised V_1 with various step numbers and notch depth level. For comparison purpose, two lines are plotted for m=7 with different d.

Table 3.1 d levels for some values of m.

m levels	3-6	7-11	12-16	17-21	22-26	27-31	32-36
d level(s)	1	2	3	4	5	6	7

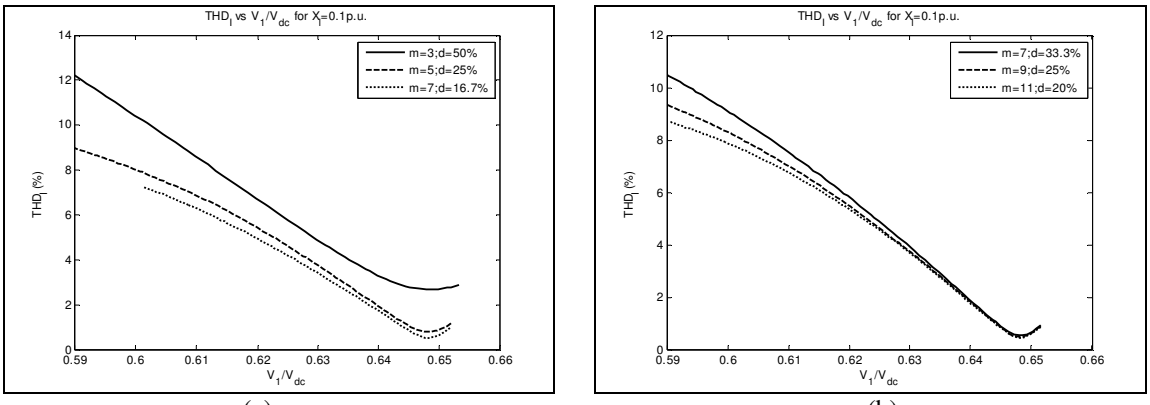


(a) (b)

Figure 3.14 Stepped MLVR-VSC voltage THD against normalised fundamental component.
(a) d = 1 step level
(b) d = 2 step level

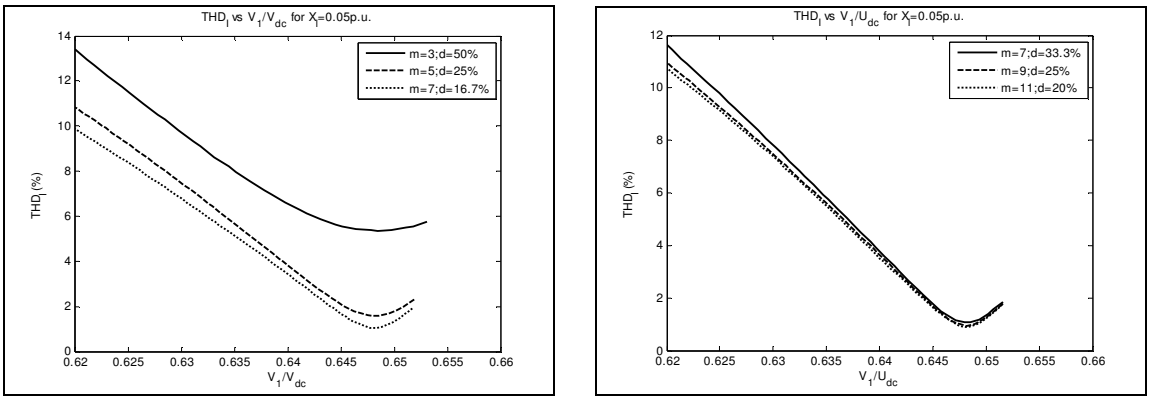
As can be seen in figure 3.14(a), when m=7 and d=1 level (i.e. 16.7%), the plotted line could not reach 10% fundamental component modulation. For both figures, the maximum saturation level for W is 25°. As the step level number increases, the discrepancies between the plots in figure 3.14(a) and 3.14(b) with ideal plots in figure 3.5 decrease. The general harmonic characteristics of ideal linear MLVR-VSC discussed before can be found in the stepped linear MLVR-VSC.

Figure 3.15 and 3.16 show the THD_I for various step number and notch depth level for two different values of x_l. As expected, the THD_I for lower x_l is higher compared to higher value of x_l.



(a) (b)

Figure 3.15 Stepped MLVR-VSC current THD for 0.1 p.u. x_l.
(a) d = 1 step level
(b) d = 2 step level



(a) (b)

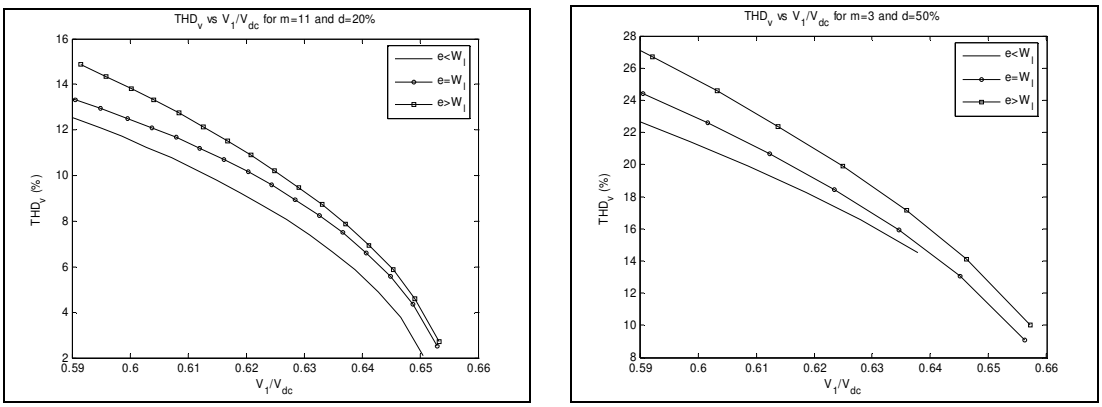
Figure 3.16 Stepped MLVR-VSC current THD for 0.05 p.u. x_l.
(a) d = 1 step level
(b) d = 2 step level

3.4.2 Width Variation of Highest and Lowest Steps

From figure 3.13, the notches in V_{YY} have the width of W and depth of d. The highest levels/platforms which occur before and after the notches are essential to provide the ZVS condition for the adjacent main bridge commutation (i.e. the highest platform in V_{YY} corresponds to the lowest platform in $V_{Y\Delta}$ and vice versa due to the complimentary restriction). Also, as shown in chapter 4, these levels/platforms are needed for the dc capacitor voltage balancing mechanism. The width of these platforms, e, are governed by the dynamics of this mechanism and the switch on(off) time of the main bridge switches. Generally, a smaller e will yield a better harmonic performance. Widths of other inclining and declining steps, W_l, shall be equal as given in

$$W_l = \frac{30° - W - 2e}{m - 2} \qquad (3.4.2.1)$$

Figure 3.17 shows the MLVR-VSC THD_V for three conditions of e.



(a) (b)

Figure 3.17 Stepped linear MLVR-VSC voltage THD for three conditions of *e*
(a) $m = 11$ and $d = 20\%$
(b) $m = 3$ and $d = 50\%$

3.5 Conclusion

Since the MLVR-VSC is intended for high power, high voltage applications, its modulation process should not compromise the advantages of ZVS, low *dV/dt* stress and ability to safely accommodate series connected power switches to withstand the high dc bus voltage. The proposed modulation method is able to preserve these advantages by notching the dc side waveforms rather than chopping the dc bus voltage via main bridge switching actions as in the case of PWM-VSC. Notched top trapezoidal waveforms, modified from the linear reinjection triangular waveform, have been adopted. The depth and width of these notches can be used to control the fundamental voltage output directly when the dc bus voltage control is not available or limited. However, a price to pay for the waveform notchings is an increase of low order harmonics at the ac side, which can only be subdued by increasing filtering effects on the ac side.

Only characteristic harmonics have been discussed in this chapter based on output waveforms obtained by assuming three phase balance, infinite dc side capacitances, zero switch on(off) time and zero voltage drops of the switches. Harmonic current penetration into the power system was investigated for worse case scenario where the reactance between the MLVR-VSC and the power system source is solely contributed by the transformer leakage reactance. Non-ideal aspects such as finite quantified waveforms and non-homogenous step width have also been discussed.

Chapter 4

Synthesis of the Varying DC waveforms

4.1 Introduction

The valves in modern high voltage converters are built with many power electronic switches connected in series. Instead of collectively clamping the series chain to one very high voltage level and firing the switches synchronously, asynchronous firing is a strategy newly proposed [11, 18 & 38]. The main concept of this strategy is to clamp the switches individually to lower voltage levels and then firing them asynchronously, in a sequential manner, to yield step-by-step varying multi-level voltage waveforms. The merits of doing so are reduced *dV/dt* stress across each switching devices and the decrease of harmonic content in the output waveform. This type of converter is named as the multi-level voltage source converter (MLVSC).

In the first sections of this chapter, brief discussions of various topologies which can be used to synthesize the multi-level waveform and their aspects are presented. The modified cascaded H-bridge topology which is used in this report to implement the MLVR-VSC is presented later. In comparison to a classic multi-level converter which needs three single pole circuits, one for each phase, MLVR-VSC only needs one phase pole of the circuit to generate the common reinjection waveforms. Additionally, voltage synthesis flexibility offered by this topology can be used to solve the capacitor balancing problem.

An observed problem with the modified cascaded H-bridge topology is that the current flow through the reinjection branch is purely ac and its relation with the main dc capacitor currents is dependent on the dc load current which is unpredictable. During real power transfer, upon multiplication with the H-bridge switching functions, it becomes either a rectifying or inverting current although the average currents into the main dc capacitors may be zero. If these charges are not transferred to and shared with the main dc capacitors, the H-bridge capacitor voltages will drift and finally lead to the failure of

the MLVR-VSC. A way to overcome this problem is to introduce a momentarily voltage sharing path between the main dc capacitors and the H-bridge capacitors. This path can be provided via the 12-pulse converter valves with some modification to their switching patterns.

4.2 Multi-level Converter Topology

Multi-level converters are a class of voltage source converters introduced recently [11, 18 & 12], with the promising advantages of low switching device ratings, good harmonic performances and capability to operate in all four quadrants of the complex power circle. The MLVSC typically synthesizes the staircase voltage waveform from several levels of dc sources. These sources can be separately powered dc sources such as battery, or output of a controlled rectifier, or simply a capacitor. The first two choices of dc source offer the advantage of balanced dc voltage sources but are very complicated and expensive to implement. The third choice offers the advantages of simplicity and low-cost but suffers greatly from unbalanced charging or discharging during steady-state and transient operation[48].

The MLVR-VSC utilises the 12-pulse converter bridge as its topological backbone. The $6k^{th}$ harmonic cancellation characteristic of the 12-pulse converter is exploited to yield the minimum harmonic content on the ac output. This leads to the MLVR-VSC dc side to be injected with $6k^{th}$ harmonic voltage components. In comparison with a classical MLVSC, which needs one pole of multi-level generating circuits to be connected to each phase of the three phase system in order to generate three phase pulsed ac voltages, the MLVR-VSC only needs one pole circuit. The multi-level topology is used to synthesize the 6 times varying dc waveforms which will be coupled onto the ac side via the 12-pulse converter bridge. Excluding the 12-pulse main bridge, the circuit elements count is reduced to a third. The discussion of multi-level generating circuits from hereon focuses only on a single pole circuit.

It is not the intention for this thesis to present in detail the operations of various MLVSC topologies. An overview of the currently available MLVSC topologies summarised from references 14 and 22 is given in Appendix B. The following subsections, however, will provide highlights of the main aspects which relate to their application in the MLVR-VSC.

4.2.1 Diode-Clamped Topology

The multi-level-diode-clamped VSC (MLDC-VSC) topology provides the output terminal with multi-level voltages via a controlled voltage divider, which divides the dc bus voltage into many equal step levels. The number of circuit elements utilised in the circuit are

$$N_{valve} = 2(m-1) \tag{4.2.1.1}$$

$$N_{diode} = (m-1)(m-2) \tag{4.2.1.2}$$

$$N_{capacitor} = (m-1) \tag{4.2.1.3}$$

where N_{valve} is the number of valves, N_{diode} is the number of diodes and $N_{capacitor}$ is the number of capacitors.

Equations 4.2.1.1-4.2.1.3 assume that the voltage rating for each element is equal to one voltage level. If series connections are required for high voltage application, then the circuit element count should be multiplied accordingly. The elements' current ratings, however, are not equal due to different total conduction time per cycle. Refer to Appendix B for details.

Conventionally, this topology suffers greatly from the capacitor voltages imbalance caused by the unequal conduction time per cycle of each switches. For the case of the MLVR-VSC, the capacitor voltages will also drift when there is active power transfer through the converter. However, the cause of the imbalance is due to the asymmetrical nature of the dc bus current rather than unequal charge or discharge time [24]. Under purely reactive power transfer, there will be no voltage balancing problem because the dc bus current is symmetrical over its half cycle time-axis. When there is active power transfer, the dc bus current becomes unsymmetrical which leads to different ampere-second product for each capacitor. This problem can be solved by modifying the firing patterns to maintain equal ampere-second product for each capacitor. The cost of this solution is a more complex control algorithm, slightly decreased harmonic performances and the limitation of the MLVR-VSC operation to low power factor.

4.2.2 Flying-Capacitor-Clamped Topology

Floating auxiliary capacitors are used in the multi-level-capacitor-clamped VSC (MLCC-VSC) to provide multi-level voltage outputs. Depending on the level number, *m*, there is an *m*-2 string of series connected auxiliary capacitors and one string of common dc bus capacitors in an MLCC-VSC. Provided the capacitors are equally rated, the total number of capacitors in an *m* level MLCC-VSC is

$$N_{capacitor} = m(m-1)/2 \qquad (4.2.2.1)$$

There are no clamping diodes used in this topology while the number of valves required is

$$N_{valve} = 2(m-1) \qquad (4.2.2.1)$$

The voltage ratings of the valves are one voltage step levels.

The voltage synthesis in MLCC-VSC has more flexibility than MLDC-VSC, because in MLCC-VSC there are multiple switching state combinations for generating a particular intermediate voltage level. The redundant combinations permit more than one current path through the capacitors; thus, by careful selection of switch state combinations, the charging and discharging effects can be evenly distributed amongst the capacitors. The selection of switch state combinations becomes very complicated when the level number is high. Nonetheless, the MLCC-VSC structure is a possible candidate to generate the required multi-level waveforms with a prospective to solve the capacitor voltage balancing problem.

The independent nature of the floating auxiliary capacitors makes it difficult to reduce their number. Therefore a large number of them are required to generate the multi-level voltages when high level number is desired.

4.2.3 Generalised bi-Logic Topology

The structure of this topology, proposed by Fang [11], is a pyramid build from generic building blocks of an MLVSC. It can be of either two or three levels. While there is only one version of a two level VSC, the three level generic VSC can be based on either MLDC-VSC or MLCC-VSC topology.

The main advantage of Fang's proposal is the ability to balance capacitor voltage in any operating condition. This is done via the path provided by the clamping switches to connect the capacitors in parallel to enforce voltage sharing between them. Also, like the MLCC-VSC, there exists switch state redundancies to synthesize the intermediate voltage levels.

Fang's proposal uses additional force commutated devices to ensure that all capacitor voltages are self-balanced all the time. However, this leads to a very large number of switches and capacitors required for high level number topology. The circuit elements required for an *m* level generalised bi-logic multi-level VSC (MLGB-VSC) are

$$N_{valve} = m(m-1) \qquad (4.2.3.1)$$

$$N_{capacitor} = m(m-1)/2 \qquad (4.2.3.2)$$

All the element voltage ratings are one voltage step level.

4.2.4 Cascaded H-bridge Topology

A single H-bridge connected to a dc source can synthesise two level bipolar voltages. By cascading many of them, it is possible to synthesise multi-level bipolar voltage waveforms.

Although (*m-1)*/2 H-bridges are able to produce an *m* stepped voltage waveform, the anti-parallel diodes in the 12-pulse converter of an MLVR-VSC prohibit the cascaded H-bridge to collectively produce negative output. Additionally, for a back-to-back connection, the chain of cascaded H-bridges has to be duplicated and then extended onto

the original chain in order to sustain the common dc bus voltage. Thus as the level number increases there is also a significant increase in circuit elements. The circuit elements required for an *m* level VSC, for back-to-back configuration, based on cascaded H-bridge topology are

$$N_{vavlve} = 8(m-1) \qquad (4.2.4.1)$$

$$N_{capacitor} = 2(m-1) \qquad (4.2.4.2)$$

Again, all the elements are rated to one voltage level. Except for the outer most H-bridges, each H-bridge capacitor is floating. Hence, they can be freely combined by force commutated devices to produce the multi-level voltage waveform. Like the MLCC-VSC, this flexibility can be utilised to solve the capacitor voltage balancing problem.

4.3 MLVR-VSC topology

Although it is possible to merge any of the multi-level topology, presented above, with the 12-pulse converter bridge to yield the MLVR-VSC, they are unsatisfactory either from technical or economical aspects. The MLDC topology is almost useless if it is to be implemented for an HVdc terminal converter due to its limitation to low power factor (in order to maintain capacitor voltage balance). The MLCC-VSC, MLGB-VSC and cascaded H-bridge topology incur a high implementation cost due to the large number of circuit elements utilised. In this section, an MLVR-VSC based on the modified cascaded H-bridge topology is presented. This modified topology inherits the synthesis flexibility of the cascaded H-bridge topology but reduces the number of circuit elements significantly.

4.3.1 Modified Cascaded H-bridge Topology

Each of the varying dc waveform shown in figure 3.2 consists of a dc component and some ac components. While the dc component can be provided by passive pre-charged capacitors, the ac components have to be synthesized by a group of actively switched dc sources.

For the linear reinjection scheme, the varying dc waveforms, $V_{YY}(\omega t)$ and $V_{Y\Delta}(\omega t)$, are complimentary to each other. The corresponding ac components in $V_{YY}(\omega t)$ and $V_{Y\Delta}(\omega t)$ have the same magnitudes but are 30° phase shifted, or half a cycle of the $1/6^{th}$ of the fundamental cycle, from each other. Hence, the ac components can be generated by a circuit common to both the 6-pulse converters: i.e. if the $V_{YY}(\omega t)$ is the sum of one passive capacitor voltage and the output of the ac waveform generating circuit, $V_{Y\Delta}(\omega t)$ would be the difference of one passive capacitor voltage and the output of the ac waveform generating circuit.

Due to its ability to generate bipolar multi-level output, the cascaded H-bridge topology was chosen as the candidate for the ac generating circuit. In reference to the summary presented in Appendix D, the original cascaded H-bridge topology has the string of H-bridges located across the dc bus and their collective operation is limited to unipolar output. Innovative to this, the string of cascaded H-bridge can be connected from the 12-pulse converter neutral point to the mid-point across the dc bus. Figure 4.1 shows the proposed MLVR-VSC topology. Note by excluding the added H-bridge chain, figure 4.1 is essentially a 12-pulse VSC. An inductor (shown in dashed line) is added deliberately in series with the cascaded H-bridges to limit current spikes during voltage sharing periods. The purpose and the mechanism of the voltage sharing are explained later in this chapter.

To simplify the description, the 6-pulse converter bridge which is connected to the Y/Y interface transformer is named as the *Y/Y main bridge* while the other 6-pulse converter is named as the *Y/Δ main bridge*. Due to historic reasons, the current path containing the ac generating circuit is named as the *reinjection branch*.

Each H-bridge capacitor in a cascade of 'n' bridges is pre-charged to a voltage level of $V_{dc}/2n$, where V_{dc} is the dc bus voltage. The dc bus capacitors, C_1 and C_2, are treated as equal and thus they acquire half the dc bus voltage. Each H-bridge has three switch states to yield three voltage levels, i.e. $-V_{dc}/2n$ (state S^{-1}), 0 (state S^0) and $V_{dc}/2n$ (state S^{+1}). Hence, it is possible to synthesize $m=2n+1$ voltage levels from a string of n cascaded H-bridges. The possible voltage levels are $-V_{dc}/2$, $-(n-1)V_{dc}/2n$, …, $-V_{dc}/2n$, 0, $V_{dc}/2n$, …, $(n-1)V_{dc}/2n$ and $V_{dc}/2$. The switch states of the H-bridges are sequentially arranged to yield a step by step varying ac *reinjection voltage* waveform, $V_r(\omega t)$. Without modulation, each step level occupies an interval of $30°/2n$.

Figure 4.2 shows an example of the voltage waveforms of an MLVR-VSC with 2 cascaded H-bridges (without modulation). The polarity reference of $V_r(\omega t)$ is taken from the 12-pulse converter neutral point to the dc bus mid point. For an MLVR-VSC with n cascaded H-bridges, the corresponding ac output voltage will be $24n$ pulsed.

With the connection shown in figure 4.1, the voltages appearing across each of the 6-pulse bridge are

$$V_{YY}(\omega t) = V_{dc}/2 + V_r(\omega t) \qquad (4.3.1.1)$$

$$V_{Y\Delta}(\omega t) = V_{dc}/2 - V_r(\omega t) \qquad (3.3.1.2)$$

When the reinjection voltage is equal to the voltage level of $V_{dc}/2$, the voltage across the Y/Δ main bridge is zero. Similarly, when $V_r(\omega t)$ is equal to $-V_{dc}/2$, the voltage across the Y/Y main bridge is zero. The 12-pulse bridge commutations are made to coincide with these zero voltage conditions so that the main valves will be zero voltage switched (ZVS). The cost, size and complexity of snubber circuits are reduced significantly because the dynamic voltage stress on the switches is minimal due to ZVS. Further, because the instantaneous power during the switching period is zero, the switching losses are negligibly small when compared to the PWM based VSCs.

Practically, for high voltage applications, the valves in the 12-pulse bridge are formed by serial connection of semiconductor devices which are individually rated much lower than the overall voltage ratings. The inherent ZVS condition in the MLVR-VSC and the step-by-step varying nature of the voltages across the main bridge valves make it possible to construct these valves with a hybrid of a few self-commutated devices and the rest of thyristors. The few self-commutated switches are used to switch-off the arm current and sustain the first increased voltage stress. Upon recovery, the thyristors will sustain the subsequent increase of voltage stress. In this case, the ZVS duration will have to be sufficiently long for the recovery of the slowest thyristors to ensure that all switchings occur within the ZVS period.

The H-bridge valves have to be constructed from self-commutated devices because they are not zero voltage switched. Presently available self-commutated devices such as GTOs, IGBTs and IGCTs are rated less than 10kV [28]. Hence, the H-bridge VSCs built from these devices, without serial connection, is limited to this range. Although H-

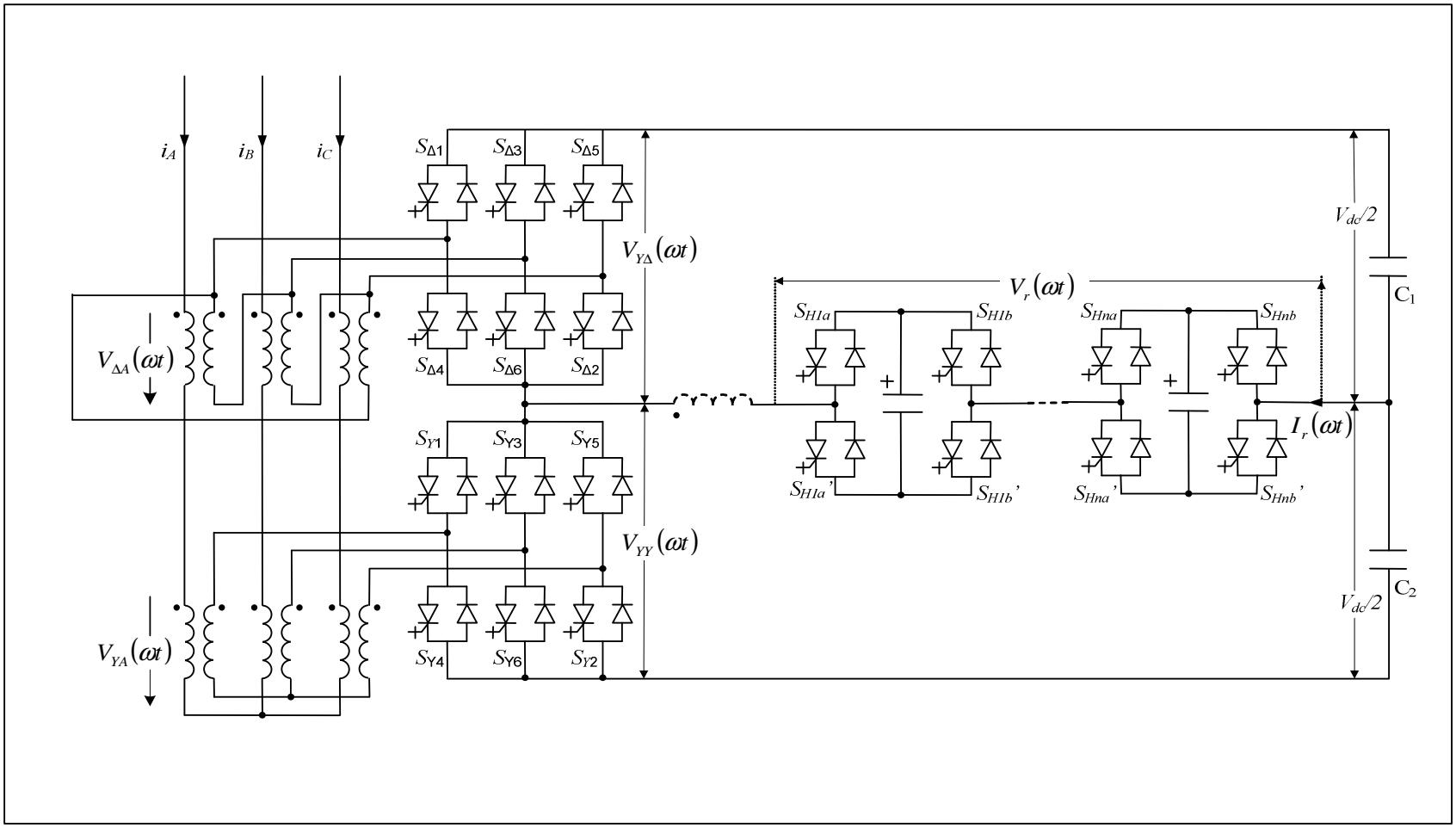


Figure 4.1 Modified Cascaded H-bridge multi-level converter (*m*-level topology)

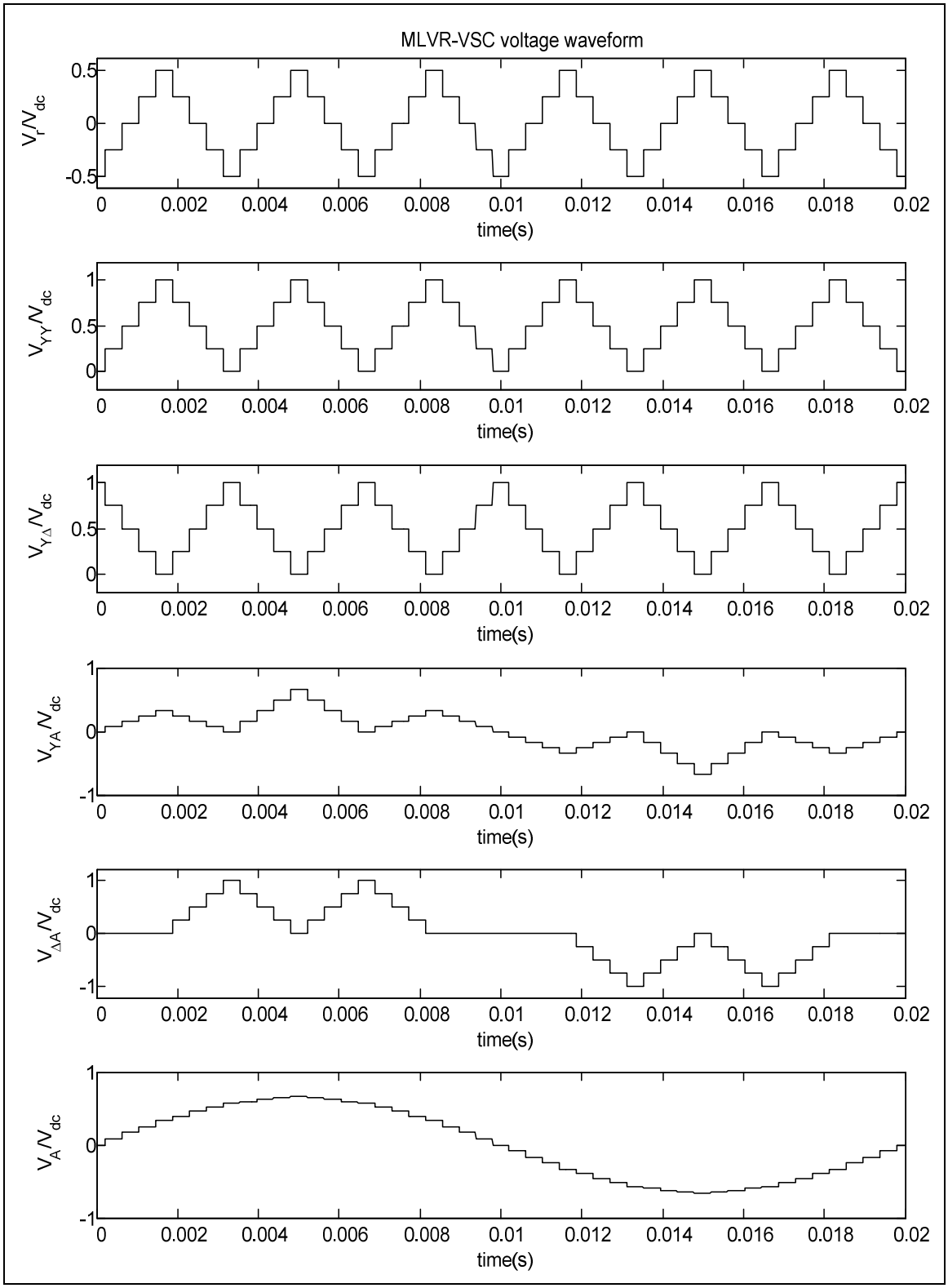


Figure 4.2 MLVR-VSC voltage waveforms with 2 cascaded H-bridge (without modulation).

bridges of high ratings can be built with these devices connected in series, the corresponding high *dV/dt* stress induced on the 12-pulse converter valves, interface transformer windings and cables can be destructive. Additionally, decreasing the number of individual H-bridges by increasing their individual ratings will decrease the waveform synthesis flexibility, which in turn limits the firing control to achieve capacitor voltage balancing.

The number of circuit elements used in this topology is reduced significantly from the original version mentioned in section 4.2.4. The main reason is that the H-bridges are now allowed to collectively synthesize negative and positive voltages. Excluding the main valves on the 12-pulse converter, the number of valves required for an *m* level MLVR-VSC is

$$N_{vavles} = 2(m-1) \qquad (4.3.1.3)$$

Excluding the dc bus capacitors, the total number of capacitors required for an *m* level MLVR-VSC is

$$N_{capacitor} = (m-1)/2 \qquad (4.3.1.4)$$

Equations 4.3.1.3 and 4.3.1.4 assume that each circuit elements are rated to one voltage step level. The 12-pulse main bridge valves and the main dc capacitors are not included because series connection of these elements is required for high voltage ratings.

Although the MLVR-VSC harmonic performance does not improve significantly after *m* becomes greater than 8, it is justifiable, from reliability point of view, to add more H-bridges onto the cascade string. Reliability of the MLVR-VSC can be increased by avoiding, as much as possible, the series connection of force commutated switches on the H-bridges. It is apparent that series connected switches are subjected to higher degrading due to higher voltage stress. Assuming that all switches and capacitors are equally rated, the component cost for more lower rated H-bridges will not be much higher than less higher rated H-bridges. Also, the cost of adding lower rated H-bridges for redundancy purpose is cheaper than adding higher rated H-bridges formed by series connected switches. The only drawback from this is the complexity increase in the firing logic and algorithm to control the H-bridge switch states.

4.3.2 Valve Switching Patterns

Distinct from the conventional 12-pulse converter based on fundamental frequency switchings, the main bridges switching functions in the MLVR-VSC have to fulfil the following objectives:

- The 12-pulse converter valves commutate under zero voltage conditions so that high voltage application is permissible;
- To provide a path to transfer powers from the reinjection branch to the main dc capacitors;
- To nullify the bulges produced complementarily by the modulation process.

As explained in chapter 3, the MLVR-VSC output voltage modulation is performed via notchings on the dc side voltage waveforms, which has lead to the notched-top trapezoidal waveform shape of $V_{YY}(\omega t)$ and $V_{Y\Delta}(\omega t)$. In order to achieve the desired modulation level, the notch width, W, is adjusted while the notch depth, d, is maintained constant. The specific level of d will depend on the topology level number, m, as depicted in table 3.1. The modulated $V_{YY}(\omega t)$ and $V_{Y\Delta}(\omega t)$ each have 12 zero voltage periods which do not fall precisely on every 30° or 60° of the fundamental cycle. Hence, in order to maintain ZVS conditions on the main valves, their commutation periods have to be shifted to coincide with the new zero voltage periods of $V_{YY}(\omega t)$ and $V_{Y\Delta}(\omega t)$.

During active power transfers, the H-bridge capacitors residing on the reinjection branch will acquire voltages unequal to those acquired by the dc main capacitors. Depending on the dc load current flow, the H-bridge capacitors can be overly charged or discharged. Hence, it is essential to occasionally provide a path for voltage sharing between the reinjection branch and the dc main capacitors to ensure that the H-bridge capacitors will track the dc bus voltage. By taking advantage of the zero voltage periods of the modulated $V_{YY}(\omega t)$ and $V_{Y\Delta}(\omega t)$, it is possible to enforce the voltage sharing through the main valves. During these periods, all the H-bridges (except the redundant ones) in the reinjection branch are either positively biased or negatively biased. By overlapping the on-states of the main bridge upper and lower valves momentarily, the reinjection branch and the dc main capacitors will form a close loop during commutation period. When

$V_r(\omega t)$ is maximum, the reinjection branch is forced to share voltage with C_1 (see figure 4.1) through the valves on Y/Δ main bridge. When $V_r(\omega t)$ is minimum, the reinjection branch is forced to share voltage with C_2 through the valves on the Y/Y main bridge.

For elaboration of this mechanism, the commutation between S_{Y1} and S_{Y4} is taken as an example. The turn-off time of the S_{Y1} is delayed while the turn-on time of S_{Y4} is advanced so that both valves will conduct together. If $|V_r(\omega t)|$ at this time is lower than the voltage drop across C_2, charge will be transferred from C_2 to the H-bridge capacitors. Similarly, if $|V_r(\omega t)|$ at this time is higher than the voltage drop across C_2, charge will be transferred from H-bridge capacitors to C_2. The duration of this overlapping period, e, is dependent on the current spikings allowed on the reinjection branch and the main valves. An inductor is deliberately added onto the reinjection branch to limit the current spike created by the initial unequal voltages of $V_r(\omega t)$ and that on C_1 or C_2.

Some of the H-bridges on the reinjection branch will be bypassed during notching. Because the reinjection branch is common to, but induces opposite voltages on, the 6-pulse main bridges, notching on $V_{YY}(\omega t)$ will cause bulging on $V_{Y\Delta}(\omega t)$ and vice versa. If these complementary bulges appear on the interface transformer secondary windings, the notches will be annihilated when the two primary winding voltages, of Y/Y and Y/Δ transformers, are summed together on the ac side. In order to avoid these complimentary bulges, either the upper or lower arms of the 6-pulse converter valves are opened to break the path connecting the reinjection branch and the dc bus capacitors. In addition, if the upper arm valves are opened, the lower arm valves are closed to provide flow path for three phase ac currents.

Figure 4.3 illustrate the dynamic switchings on the 12-pulse converter valves against conventional 180° firings. It can be seen that the switching frequency of the main valves have now increased from one per cycle to three per cycle.

At any instant of time, two of the valves on each H-bridge are turned-on. Compliment annotation of H-bridge valves as shown in figure 4.1 implies that turning on one of the switches pair will exclude the other from being switched on. Each H-bridge is capable of generating bipolar output voltage: state S^{+1} corresponds to turning on of S_{Hna} and S_{Hnb}' and contribute positively to $V_r(\omega t)$; state S^{-1} corresponds to turning on of S_{Hna}' and S_{Hnb} and contribute negatively to $V_r(\omega t)$; state S^0 corresponds to turning on of either S_{Hna} and

S_{Hnb} or S_{Hna}' and S_{Hnb}'. This state will bypass the H-bridge and contribute nothing to $V_r(\omega t)$.

For the period $W/2<\omega t<\pi/6-W/2$, the H-bridges are biased positively one by one in steps of $V_r(\omega t)$ from minimum value of $-V_{dc}/2$ to maximum value of $V_{dc}/2$. For the period $\pi/6+W/2<\omega t<\pi/3-W/2$, the H-bridges are biased negatively one by one in steps of $V_r(\omega t)$ from maximum value of $V_{dc}/2$ to minimum value of $-V_{dc}/2$. In order to create the notches for the modulation process, a number of H-bridges are bypassed.

Figure 4.4 illustrate the H-bridge valve switching functions for the MLVR-VSC with one H-bridge. At periods around 0, $\pi/6$, $\pi/3$, …, 2π, the H-bridge is bypassed to create the modulation notches. Either the upper arms or the lower arms of the 6-pulse main bridge with complementary bulges are opened or closed. Prior to and after these notches, valves on the main bridges commutate with zero voltage. Voltage sharing between the reinjection branch and dc bus capacitors is enforced during zero voltage conditions by overlapping on states of both upper and lower arm valves on one phase leg. The MLVR-VSC output voltages for the switching function shown in figure 4.3 and 4.4 are illustrated in figure 4.5.

4.3.3 H-bridge Switch States and Capacitor Voltage Balancing

Except for the highest and lowest step levels and for the single H-bridge topology, there is more than one switch state combination which can produce the voltage levels on the reinjection voltage, $V_r(\omega t)$. As $V_r(\omega t)$ approaches mid level, i.e. zero voltage, the synthesis flexibility grows to a maximum number of possible switch state combinations. Table 4.1 lists all the switch state combinations to synthesize various levels of $V_r(\omega t)$ for an MLVR-VSC with 3 cascaded H-bridges. Only two valves of each H-bridge are shown. The other valves switch states can be determined by the complimentary rule. Note that it is prohibited for both valves in a complimentary pair to conduct together; otherwise, the dc sources (H-bridge capacitors in this case) will be short-circuited.

Only one set of the H-bridges' switch state combination sequences needs to be repeated over every 60° to yield the step-by-step varying $V_r(\omega t)$ if the dc sources are built from batteries or controlled rectifiers. In such cases, the voltage drops across the H-bridges

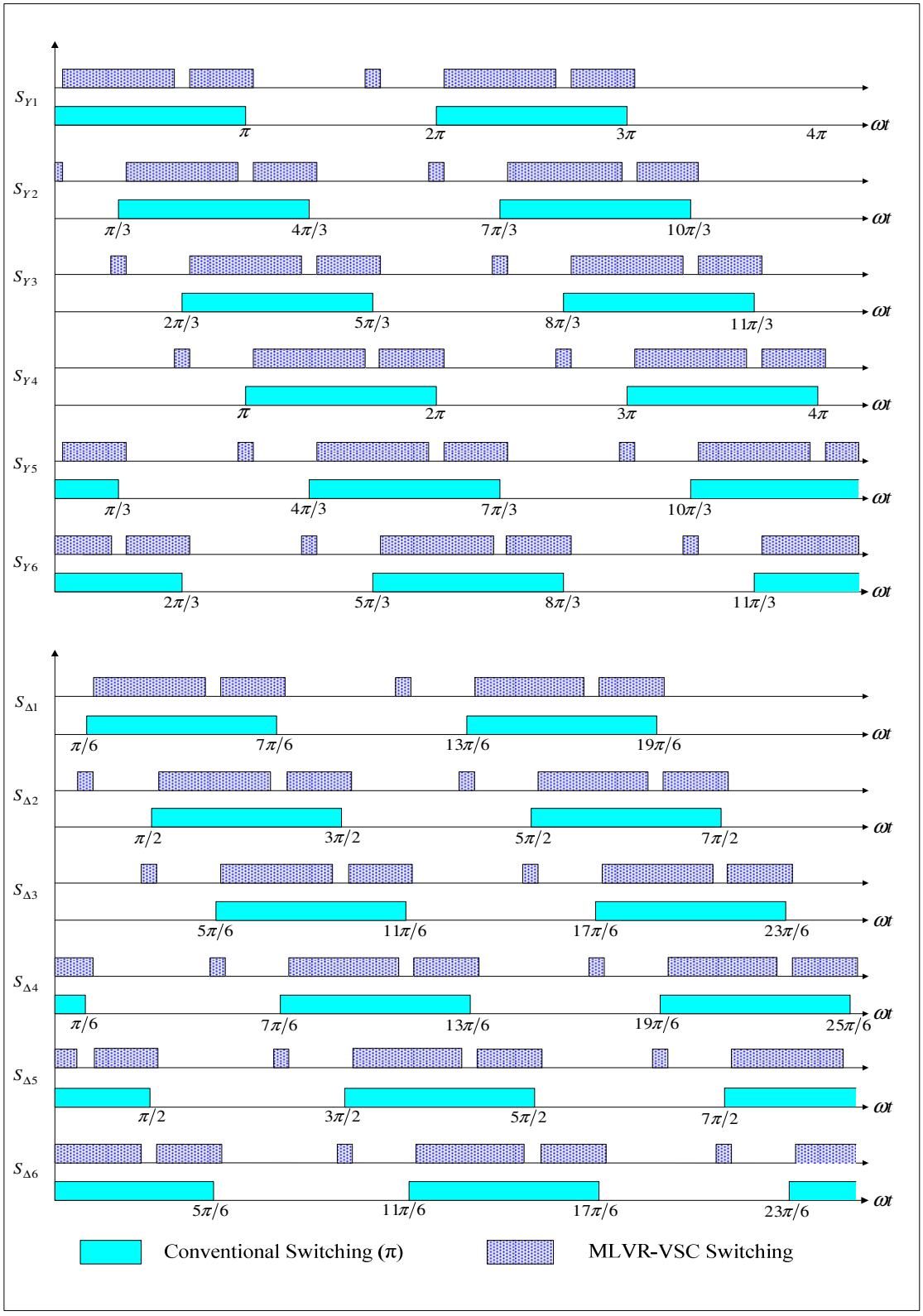


Figure 4.3 12-pulse converter main bridge switchings in MLVR-VSC

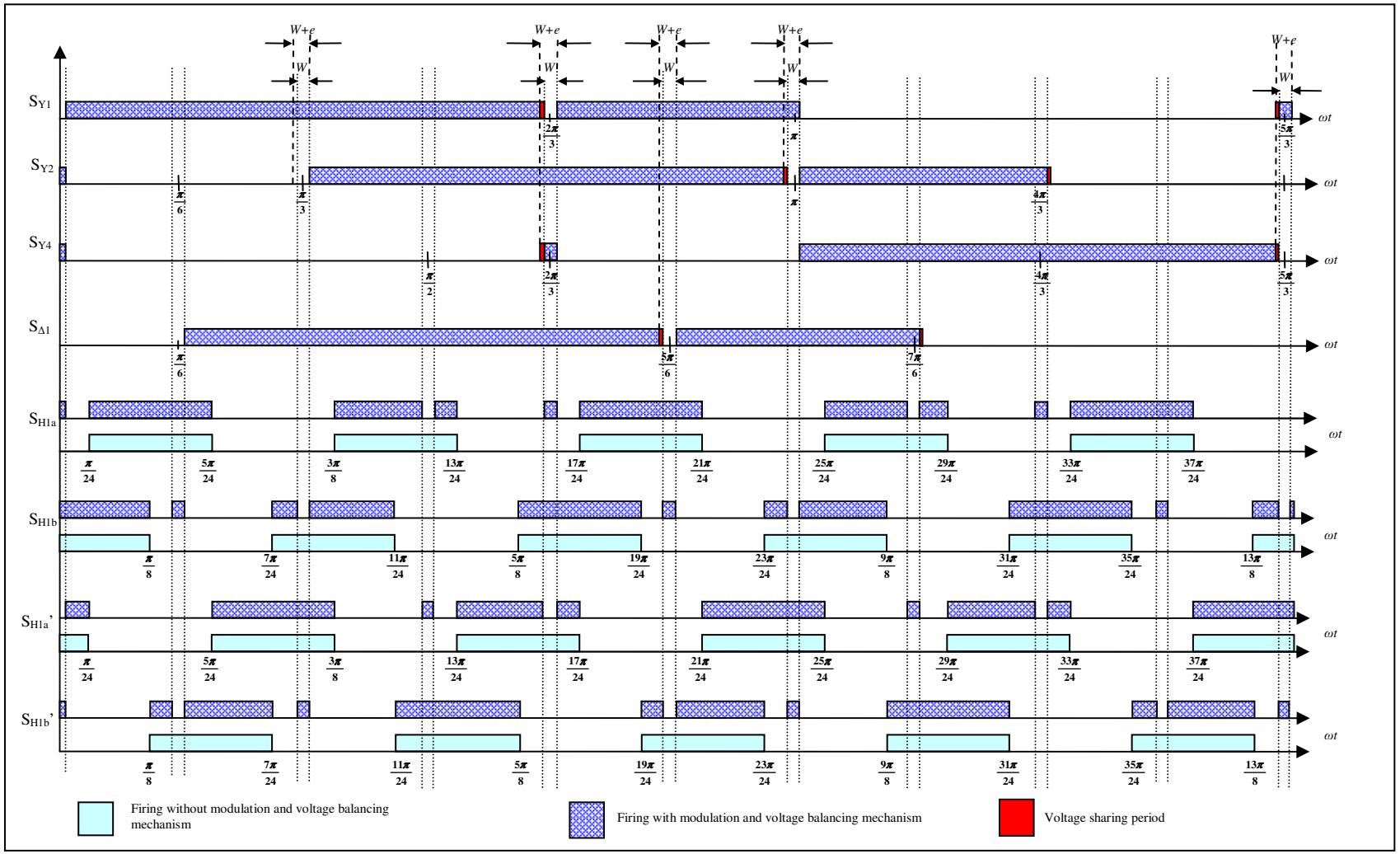


Figure 4.4 H-bridge valves switchings for an MLVR-VSC with one H-bridge.

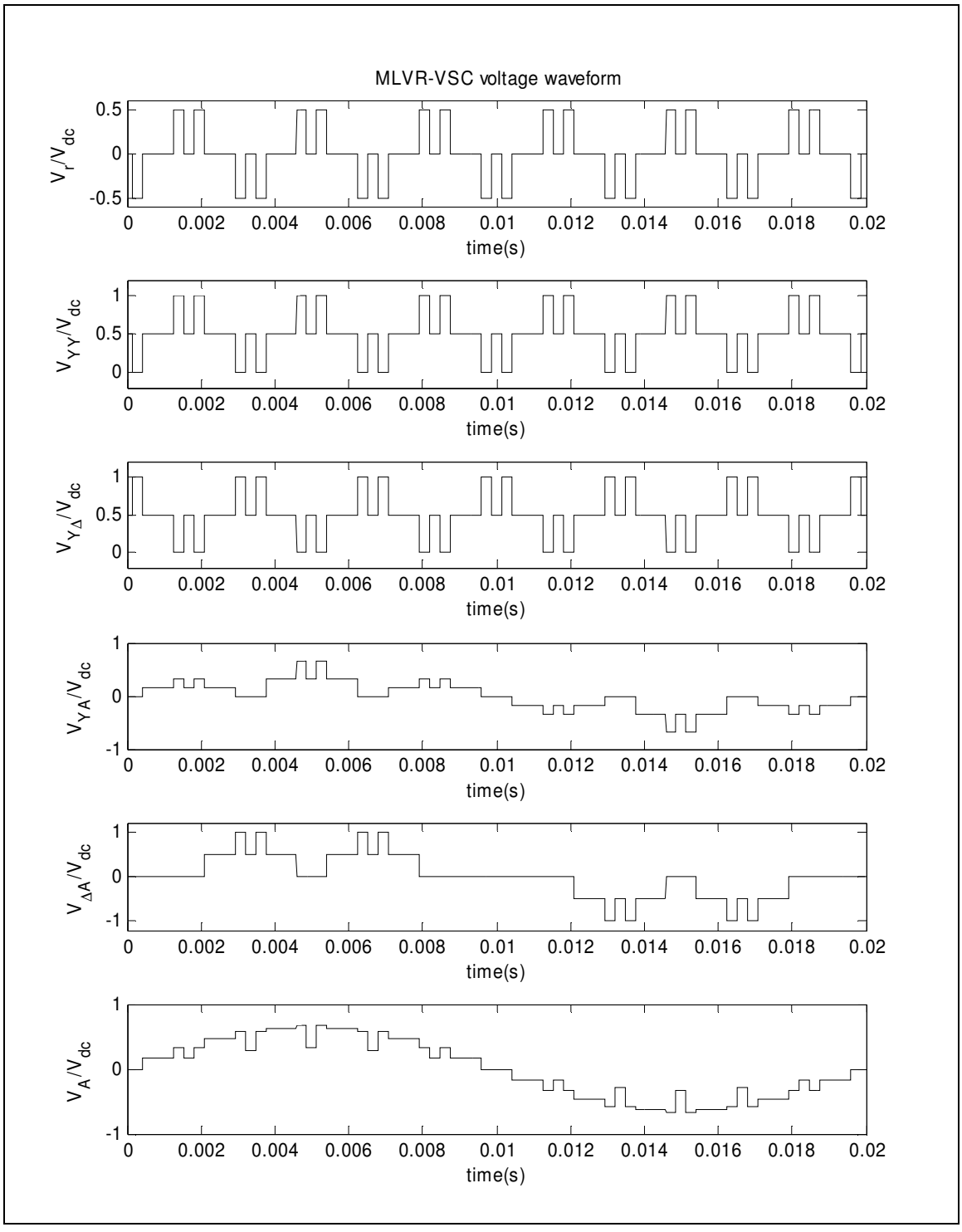


Figure 4.5 MLVR-VSC modulated voltage waveforms based on one H-bridge topology.

will not be affected by the reinjection current flow. Unfortunately, this is not the case usually where the H-bridges in VSCs are built with cheaper and less complex finite capacitors. Except for perfectly zero power factor converter operation, the reinjection current is asymmetry about the half period (of the 1/6 of the fundamental period) time-axis. Also, the uneven negatively and positively biased periods of each H-bridge will cause the capacitors to acquire different voltages over every 60°. Hence, each step level cannot be synthesized by one switch state combination alone.

While the synthesis flexibility is a feature which can be exploited to achieve H-bridge capacitor voltage balancing, it is a tedious task to choose the appropriate combination in order to evenly distribute the reinjection currents between the H-bridge capacitors. The simplest analogy for topology of any level number is to rotate the states of each H-bridge to occupy different parts of a 60° cycle over some number of cycles until all the individual capacitor average currents are equal for one rotation. However, uncontrollable circumstances such as transients and three phase unbalance can defy this primitive algorithm; hence, there is a need for a more sophisticated algorithm with self-deterministic capability. However, because the charging and discharging effects of capacitors differ for each level number topology, the H-bridge capacitor voltage balancing algorithm would be specific for each level number topology. In addition, the outcome of switch-state combination, deduced by the algorithm, should require the least switching frequencies from the switches. For these reasons, this matter is not investigated in this report and the MLVR-VSC simulation results, which are presented in chapter 5, are based on one H-bridge topology.

4.4 Current Paths of MLVR-VSC

4.4.1 AC Current Paths

Following the 12-pulse converter switch pattern change as shown in figure 4.3 and figure 4.4, the ac current paths on the 12-pulse converter change considerably. In addition to the conventional conduction paths, of either two upper arms valves and one lower arm valve or one upper arm valve and two lower arms valves, there are two more ac current conduction patterns for each 6-pulses main bridge. One occurs during the voltage sharing

Table 4.1 Switch states of an MLVR-VSC based on 3 cascaded H-bridge

Output Voltage	Capacitor Path**	Switch-state*					
		S_{H1a}	S_{H1b}	S_{H2a}	S_{H2b}	S_{H3a}	S_{H3b}
$-V_{dc}/2$	$-C_{H1}-C_{H2}-C_{H3}$	0	1	0	1	0	1
$-V_{dc}/3$	$-C_{H1}-C_{H2}$	0	1	0	1	1/0	1/0
	$-C_{H1}-C_{H3}$	0	1	1/0	1/0	0	1
	$-C_{H2}-C_{H3}$	1/0	1/0	0	1	0	1
$-V_{dc}/6$	$-C_{H1}$	0	1	1/0	1/0	1/0	1/0
	$-C_{H2}$	1/0	1/0	0	1	1/0	1/0
	$-C_{H3}$	1/0	1/0	1/0	1/0	0	1
	$-C_{H1}+C_{H2}-C_{H3}$	0	1	1	0	0	1
	$-C_{H1}-C_{H2}+C_{H3}$	0	1	0	1	1	0
	$+C_{H1}-C_{H2}-C_{H3}$	1	0	0	1	0	1
0	None	1/0	1/0	1/0	1/0	1/0	1/0
	$+C_{H1}-C_{H2}$	1	0	0	1	1/0	1/0
	$+C_{H1}-C_{H3}$	1	0	1/0	1/0	0	1
	$+C_{H2}-C_{H3}$	1/0	1/0	1	0	0	1
	$-C_{H1}+C_{H2}$	0	1	1	0	1/0	1/0
	$-C_{H1}+C_{H3}$	0	1	1/0	1/0	1	0
	$-C_{H2}+C_{H3}$	1/0	1/0	0	1	1	0
$V_{dc}/6$	$+C_{H1}$	1	0	1/0	1/0	1/0	1/0
	$+C_{H2}$	1/0	1/0	1	0	1/0	1/0
	$+C_{H3}$	1/0	1/0	1/0	1/0	1	0
	$+C_{H1}-C_{H2}+C_{H3}$	1	0	0	1	1	0
	$+C_{H1}+C_{H2}-C_{H3}$	1	0	1	0	0	1
	$-C_{H1}+C_{H2}+C_{H3}$	0	1	1	0	1	0
$V_{dc}/3$	$+C_{H1}+C_{H2}$	1	0	1	0	1/0	1/0
	$+C_{H1}+C_{H3}$	1	0	1/0	1/0	1	0
	$+C_{H2}+C_{H3}$	1/0	1/0	1	0	1	0
$V_{dc}/2$	$+C_{H1}+C_{H2}+C_{H3}$	1	0	1	0	1	0

*Only two valves of each H-bridge are shown. The states of the adjacent switches can be determined from the complimentary rule. Also, switch state 1/0 implies that H-bridge is bypassed. During this state, the switch can either be on or off but the state of the switch pair must be the same, i.e. if S_{Hna}=1 then S_{Hnb}=1 or if S_{Hna}=0 then S_{Hnb}=0.

**"+" sign indicate current flow into capacitor,"-" sign indicates current flow out of capacitor.

between the reinjection branch and the dc bus capacitors while the other occurs when the complimentary bulges are prevented from being reflected onto the ac side.

During both of these periods, the three phase ac currents will circulate within the valves. If the three phase currents are perfectly balanced, they will cancel out each other before reaching the terminals connected to the dc bus. Either all the valves on the upper arms or lower arms of all three phases are closed.

During the voltage sharing period, not only is there a bypass path for the three phase ac currents, the dc current is bypassed as well. While this may sound disastrous, it is not prohibitive when the voltage across the 6-pulse converter bridge is almost zero and an inductor is added on the reinjection branch to limit the current spike create by this small voltage drop.

Figure 4.6 gives an illustration of the ac current paths on the 12-pulse converter bridge. From period $-W/2$ to $W/2$, the complimentary bulge appears on the Y/Y main bridge. Hence, S_{Y2}, S_{Y4} and S_{Y6} are turned on while the Y/Δ main bridge maintains normal operation. It is vital to keep S_{Y1}, S_{Y3} and S_{Y5} opened at this period; otherwise, C_2 will discharge to the reinjection branch. During period $W/2$ to $\pi/6-W/2-e$, both the 6-pulse bridges maintain normal operation. From period $\pi/6-W/2-e$ to $\pi/6-W/2$, $V_r(\omega t)$ has reached its maximum and voltage sharing between the reinjection branch and C_1 is desirable. Hence, $S_{\Delta 2}$, $S_{\Delta 4}$, $S_{\Delta 6}$ and $S_{\Delta 5}$ are turned on to provide both ac and dc side bypasses. The ac current conduction paths will follow similar patterns with a total of 6 voltage sharing periods and 6 complimentary bulges elimination for each 6-pulse bridge in one cycle. The ac current bypass is alternately provided by the upper and lower arms while the voltage sharing bypass is alternately provided by each phase leg of the 6-pulse main bridges.

4.4.2 DC Side Current Paths of MLVR-VSC

For a balanced system, the MLVR-VSC dc side waveforms are identical for every 60° of a fundamental cycle. The Y/Δ main bridge dc side waveforms are repetitive over every alternate 60° for periods of $-30°<\omega t<30°$, $30°<\omega t<90°$, $90°<\omega t<150°$ etc. The Y/Y main bridge dc side waveforms are repetitive for every alternate 60° for periods of $0°<\omega t<60°$, $60°<\omega t<120°$, $120°<\omega t<180°$ etc. Additionally, the Y/Δ main bridge and Y/Y main bridge dc side waveforms are identical except that they are 30° phase-shifted from each

other. For these reasons, the dc side conduction paths presented here are based on the analysis for period from 0° to 60°, but they are valid for any other periods of time.

There are a total of 6 stages (a to f) of dc side conduction paths in every 60° of MLVR-VSC operation. The illustrated dc side current conduction paths for period of $0°<\omega t<60°$ in figure 4.7 collectively represent the H-bridges residing on the reinjection branch with one dc capacitor. Polarity for this capacitor is indicated only for voltage sharing periods where the reinjection voltage $V_r(\omega t)$ is at its maximum or minimum. Other stages where the polarity is not marked for this capacitor indicate that the H-bridges are switched sequentially to synthesize the stepped ac varying $V_r(\omega t)$.

Ac current bypass actions of the Y/Y and Y/ Δ main bridge, where either all upper arms valves are closed and all lower arms valves are opened or all lower arms valves are closed and all upper arms valves are opened, will be seen as an open circuit by the MLVR-VSC dc side currents. Voltage sharing periods where the reinjection H-bridges capacitors are forced to transfer charges to either of the dc main capacitors, C_1 or C_2, are seen as short-circuits by the MLVR-VSC dc side currents. The blocks with embedded GTOs in figure 4.7 represent the conventional operation of the main bridge. The three phase MLVR-VSC ac output currents are represented as in equation 3.3.2.5. Dc load of the converter is simply represented as a dc current source across the dc bus.

The open circuit conditions for the Y/Y main bridge in stage a and the Y/Δ main bridge in stage d have cause the main bridge dc currents to be diverted into the reinjection branch (i.e. when Y/Y main bridge is opened while Y/Δ main bridge operates conventionally, the Y/Δ main bridge dc side current has to flow through the reinjection branch in order to complete the loop). This indicates that the reinjection branch circuit elements have to carry the same rated current as the main bridge valves during notching periods.

Although the H-bridges have to be sequentially switched to synthesize multi-level $V_r(\omega t)$ without zero voltage conditions, the switching losses in the reinjection branch are still much lower than the switching losses of the PWM schemes, because the voltage stress across the H-bridge valves is a fraction of the dc bus voltage. The snubbers associated with the H-bridge valves have to be large enough to absorb the release energy associated with these switching actions.

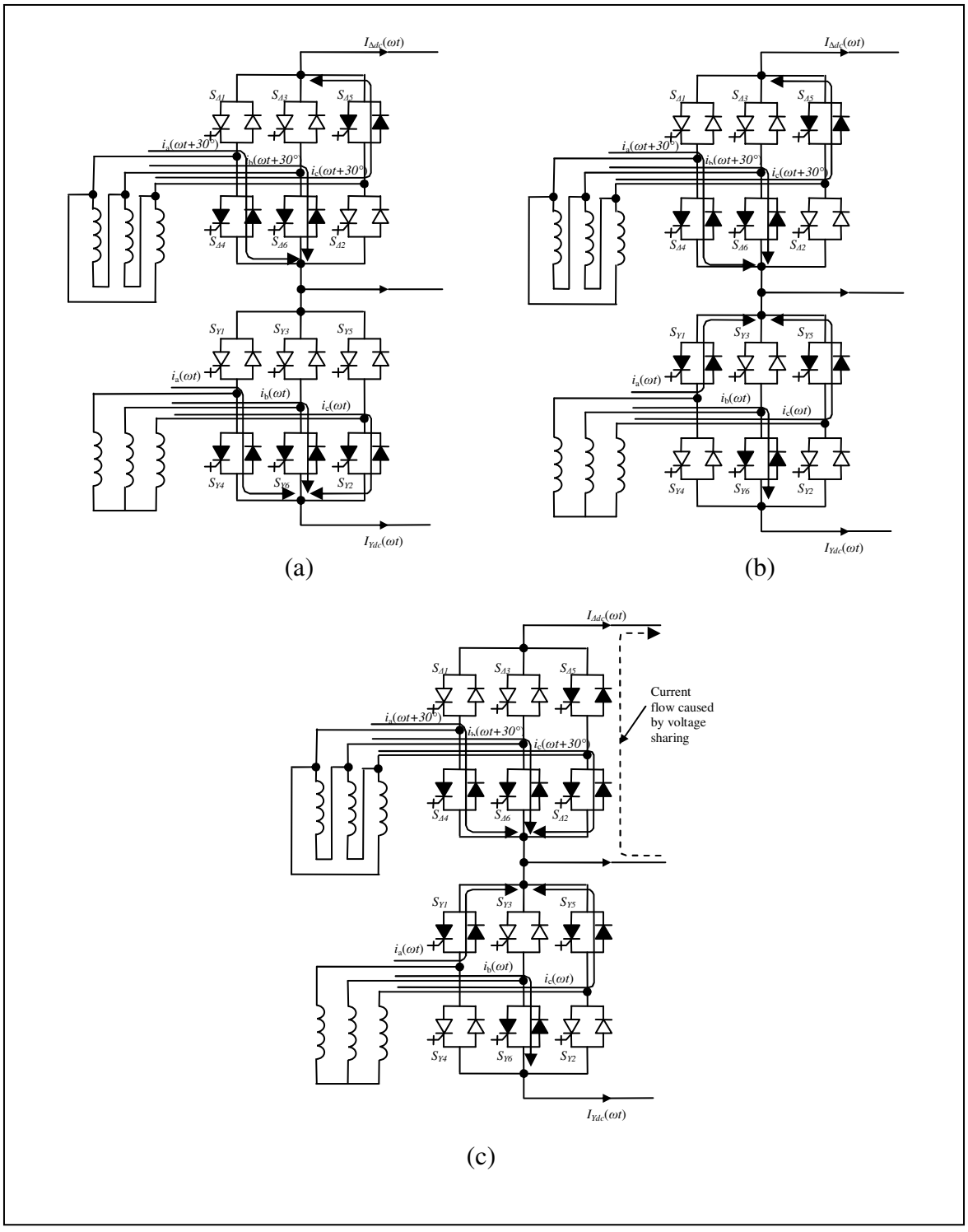


Figure 4.6 AC currents paths of the 12-pulse converter bridge.

(a) period for $-W/2 < \omega t < W/2$;

(b) period for $W/2 < \omega t < \pi/6\text{-}W/2\text{-}e$;

(c) period for $\pi/6\text{-}W/2\text{-}e < \omega t < \pi/6\text{-}W/2$.

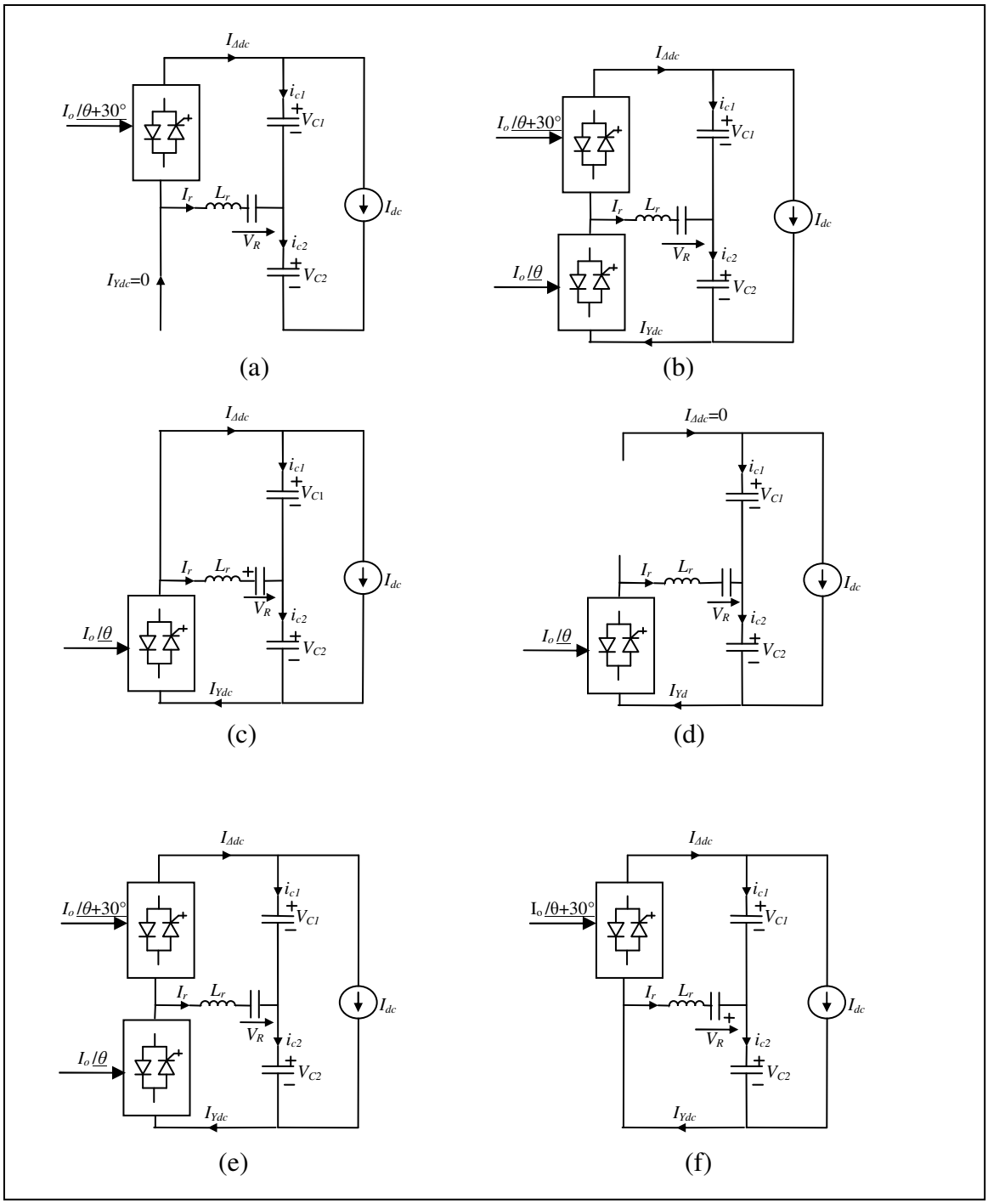


Figure 4.7. DC side conduction state of the MLVR-VCS.

(a) Period for $-W/2<\omega t<W/2$;
(b) Period for $W/2<\omega t<\pi/6-W/2-e$
(c) Period for $\pi/6-W/2-e<\omega t<\pi/6-W/2$;
(d) Period for $\pi/6-W/2<\omega t<\pi/6+W/2$;
(e) Period for $\pi/6+W/2<\omega t<\pi/3-W/2-e$;
(f) Period for $\pi/3-W/2-e<\omega t<\pi/3-W/2$.

4.4.3 Special Conduction Path if $|V_r|>V_{C1}$ or $|V_r|>V_{C2}$

Amongst all the conduction paths presented in the section 4.4.1 and section 4.4.2, the $|V_r|$ will reach maximum for some fraction of period during stages b, shown figure 4.6, for ac side currents, and b and e, shown figure 4.7, for dc side currents. Should $|V_r|$ becomes greater than V_{C1} or V_{C2} during these fraction periods, the main bridges anti-parallel diodes will be forward-biased. The choice of which main bridge diodes are forward-biased is dependent on the polarity of V_r, i.e. if V_r is positive and $|V_r|>V_{C1}$ then Y/Δ main bridge diodes will be forward biased to transfer charges from the reinjection branch to capacitor C_1, if V_r is negative and $|V_r|>V_{C2}$ then Y/Y main bridge diodes will be forward biased to transfer charges from the reinjection branch to capacitor C_2.

The occurrence of the special conduction paths is not controllable and hence not desirable from a control point of view. However, the ac current flow, shown in figure 4.8, during these special conditions is not disrupted. Depending on their direction, the ac currents will either circulate in the main bridge valves or flow through the dc capacitors. The difference of $|V_r|-V_{C1}$ and $|V_r|-V_{C2}$ is kept to a small value with the voltage sharing mechanism. Because the diodes only allow uni-direction current flow, this special conduction path is broken when $|V_r|$ becomes smaller than V_{C1} or V_{C2}. The duration of this special condition is very small.

4.5 Conclusion

In this chapter, the modified cascaded H-bridge topology is proposed to generate the injected harmonics (onto the dc bus) as required by the reinjection concept. Amongst many aspects of this topology, the most distinct advantage is the reduced number of circuit elements used when compared against other multi-level topologies. Other advantages are inherited from the multi-level converters and the reinjection concept such as zero voltage commutation of the main bridges, low dynamic (dV/dt) voltage stress, reduced harmonic content and capability to operate in all four quadrants of the complex power circle.

Two main issues have been resolved so that the proposed MLVR-VSC topology can function properly and embrace the voltage modulation feature. One issue is the

complementary bulges (a side effect from the fact that the two 6-pulse main bridges are complementary to each other) which must be eliminated before the dc side waveforms are coupled onto the ac side. The other issue is the tracking of the reinjection voltage to the dc bus voltage. Both of these issues are resolved by modifying the switching functions of the main bridges. This has resulted in the increase of main bridge valves switching frequency from once per cycle to three times per cycle. Also, an inductor is deliberately added onto the reinjection branch to limit current spikes during voltage sharing between the H-bridges and the dc bus main capacitors.

Analytical current flows within the converter presented here show that there are two additional stages for each of the ac side and dc side current flows. The ac currents always continue to flow, in one way or another, either through the dc bus or just circulating through the main bridge. This continuity is based on the assumption that the inductances present on the ac side are much more significant than those present on the dc side. An observation made during the dc side current flow analysis is that when the complementary bulge is eliminated via main bridge switching functions, the main bridge current is diverted into the reinjection branch. This will lead to the increase current ratings of the reinjection branch circuit elements.

When more than one H-bridge is added onto the reinjection branch to yield more voltage step levels (thus improving the converter harmonic performance), the balance of voltages of the H-bridges can be an issue. This is of concern when the H-bridge dc sources are implemented with finite capacitors and the converter is operating at other than zero power factor. The different charging effects of each H-bridge capacitor by asymmetrical currents during non-zero power factor operation are dependent on the time when the H-bridge is fired. A possible way to solve this problem is to carefully arrange the H-bridge switch state combination sequence so that the reinjection current can be evenly distributed among the capacitors. However, due to time limitation, this work has not been performed; which has lead to the single H-bridge MLVR-VSC model being used in simulations. The simulations result for a single H-bridge MLVR-VSC are presented and discussed in chapter 5.

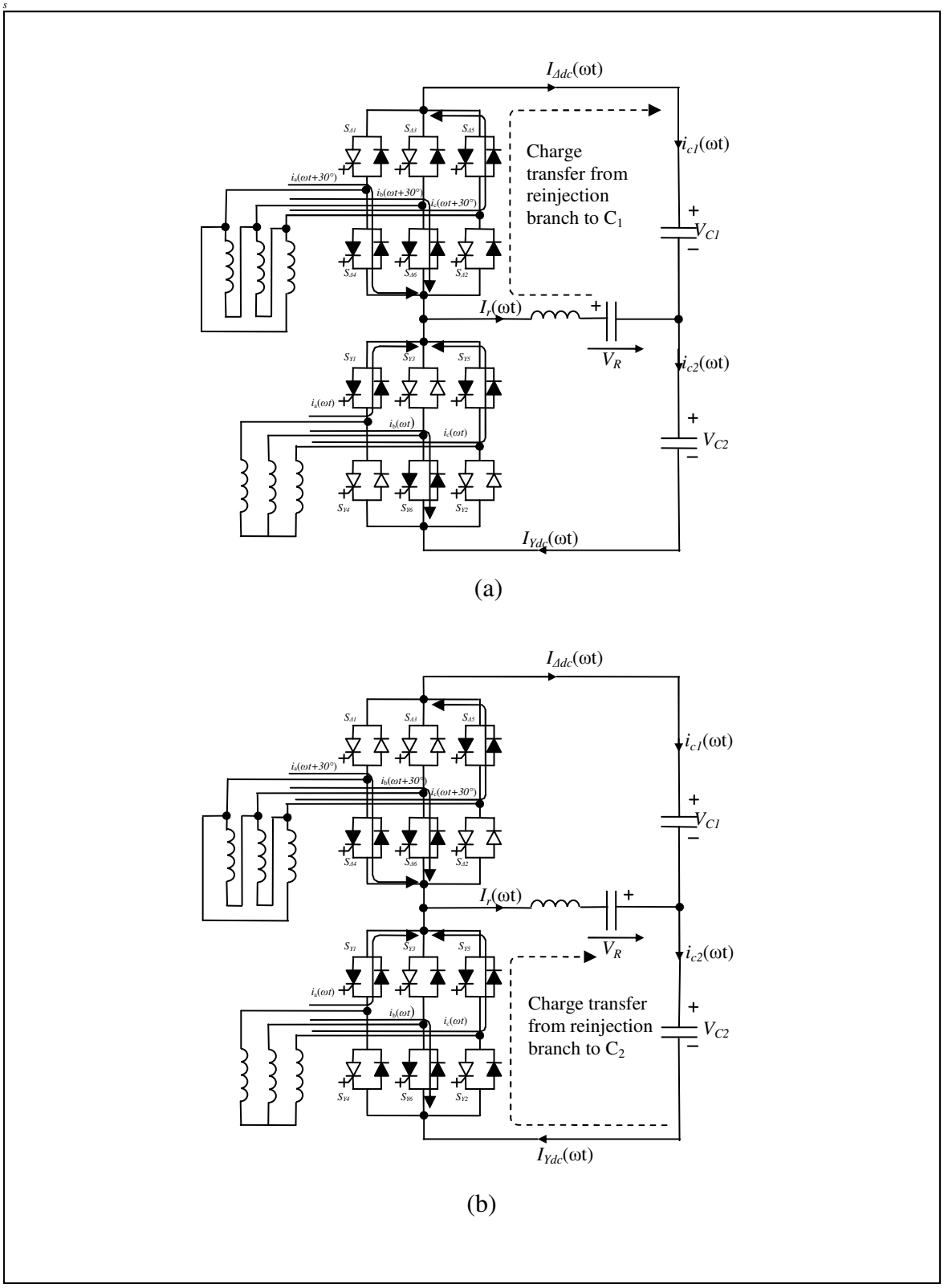


Figure 4.8 Special conduction paths
(a) $|V_r|>V_{C1}$, charge transfer from the reinjection branch to C_1;
(b) $|V_r|>V_{C2}$, charge transfer from the reinjection branch to C_2.

Chapter 5

Simulation studies and Control Strategy

5.1 Introduction

The terminals of a HVdc transmission system are connected to power systems with different characteristics and hence are subjected to different compensation requirements during both steady-state and transient events. This has initiated the research for a more controllable ac/dc converter to be implemented at its terminal. Although an HVdc link based on the reinjection concept, proposed in references 26&27, has many advantages, one of its limitation is that reactive power generated at the terminals is strictly related to the globally shared dc bus voltage. Previous chapters have presented a method to enhance the MLVR-VSC with a limited voltage modulation capability and also the topology used to realise this method.

The purpose of this chapter is to verify and investigate the use of modulated MLVR-VSCs for back-to-back configured HVdc applications. Prior to this, however, the philosophy and system to control the MLVR-VSCs' operations have to be studied. Also, the MLVR-VSC operating on a stand-alone basis has to be verified in order to provide some justification to the analysis discussed in chapters 3 and 4.

The safe operation margins and steady-state operation regions of the HVdc link are determined by studying the phasor relationships between fundamental components. The control model for the link is analysed for the steady-state conditions. Firing logics and control loops deduced using these findings are presented in this chapter.

In the last sections of this chapter, waveforms simulated using the EMTDC-PSCAD platform are discussed. The verifications determine the HVdc link dynamic control performance, active and reactive power flow control flexibility.

5.2 Back-to-back MLVR-VSC Model

The single H-bridge MLVR-VSC topology, introduced in chapter 4, is used here as the basis for a back-to-back VSC (BTB-VSC) link. In order to reduce the switching losses, as described in chapter 4, the main bridge switches commutate under zero voltage condition. The notching of waveforms is performed via the switching functions of the H-bridge together with some modification to the main bridge switching functions. The two converters share the same main dc capacitors, C_1 and C_2, and hence link the two converters in back-to-back fashion, while each has a single H-bridge residing on its reinjection branch. A simplified model of the BTB-VSC link is shown in figure 5.1. Each converter block represents a single H-bridge MLVR-VSC excluding the main dc capacitors. This test system is used to investigate active power transfer and independent reactive power generation control.

5.2.1 The Control Model of the Back-to-back MLVR-VSC

The high level control of the BTB-VSC link has to be developed taking into account the limitation of independent amplitude control of the converter voltage fundamental component. In the BTB-VSC link there are only four input parameters for the dual converters. Two are the phase angle difference between the converter output voltages and their respective source voltages. The other two are the modulation notch widths of the respective converter output voltage waveforms.

The control model of the dual converter system is developed with reference to the model shown in figure 5.1, where the active and reactive powers are viewed as output parameters while the dc bus voltage is viewed as an intermediate parameter of the system. Under the assumption of balanced operation, the interface transformers are modelled by their fundamental leakage reactances X_{l1} and X_{l2}. Through these two reactors the dual converter system is connected to two infinite buses, which are modelled by ideal voltage sources with RMS voltage V_{S1} (at 60Hz) and V_{S2} (at 50Hz). The converters are modelled by their output voltage components at fundamental frequency. Using the converter voltages as reference, ϕ_1 and ϕ_2 are the phase angle displacements of the power system sources. The ac side current reference directions are taken as into the converter. The dc currents, I_{dc1} and I_{dc2}, are the average value of Y/Δ main bridge dc side currents ($I_{\Delta dc}$). The shared dc bus voltage is denoted as V_{dc}.

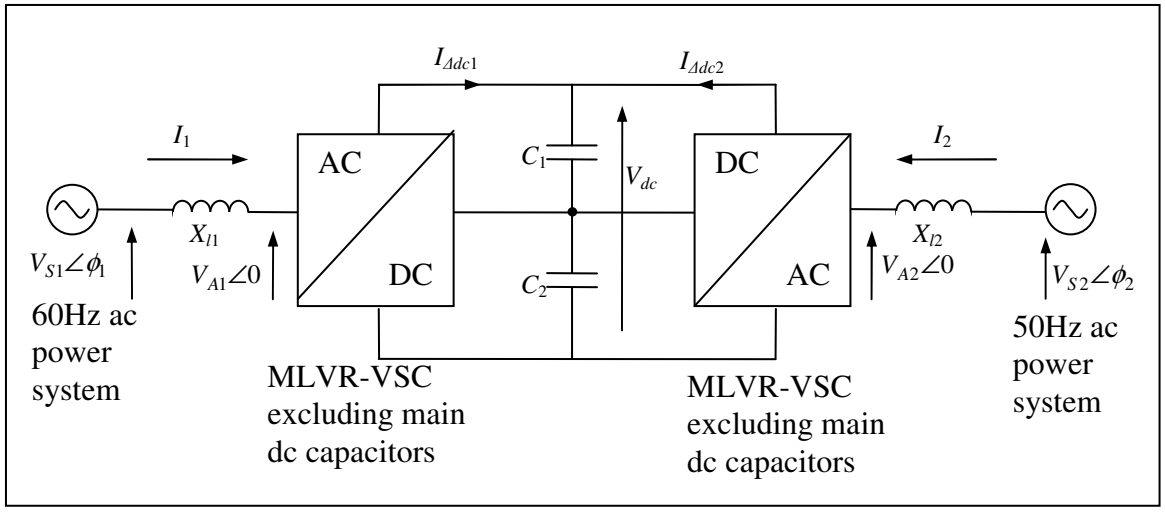


Figure 5.1 BTB-VSC Link model

Based on the model in figure 5.1, the following formulas can be deduced:

$$P_1 = \frac{3V_{S1}V_{A1}}{X_{l1}}\sin(\phi_1) \qquad P_2 = \frac{3V_{S2}V_{A2}}{X_{l2}}\sin(\phi_2) \qquad (5.2.1.1)$$

$$Q_1 = \frac{3V_{S1}V_{A1}}{X_{l1}}\cos(\phi_1) - \frac{3V_{S1}^2}{X_{l1}} \qquad Q_1 = \frac{3V_{S2}V_{A2}}{X_{l2}}\cos(\phi_2) - \frac{3V_{S2}^2}{X_{l2}} \quad (5.2.1.2)$$

$$I_{dc1} = [I_{\Delta dc1}]_{avg} = (P_1 - P_{L1})/V_{dc} \qquad I_{dc2} = [I_{\Delta dc2}]_{avg} = (P_2 - P_{L2})/V_{dc} \quad (5.2.1.3)$$

$$V_{dc} = \left(\frac{1}{C_1} + \frac{1}{C_2}\right)\int (I_{\Delta dc1} + I_{\Delta dc2})dt = \frac{1}{C}\int (I_{\Delta dc1} + I_{\Delta dc2})dt \qquad (5.2.1.4)$$

Where P_1 and P_2 are the real powers transferred from the 60Hz and the 50Hz power systems to the converters, P_{L1} and P_{L2} are the losses in the two converters, and Q_1 and Q_2 are the reactive powers generated by the two converters respectively. The converter fundamental output voltage relation to V_{dc} is dependent on the notch width (W), depth (d) and number of step levels, equation 3.3.1.1 gives this relationship for ideal waveform with infinite step level number. For finite step level number, in this case a single H-bridge MLVR-VSC will yield ac voltage waveforms with 24 pulses, equation 3.3.1.1 can

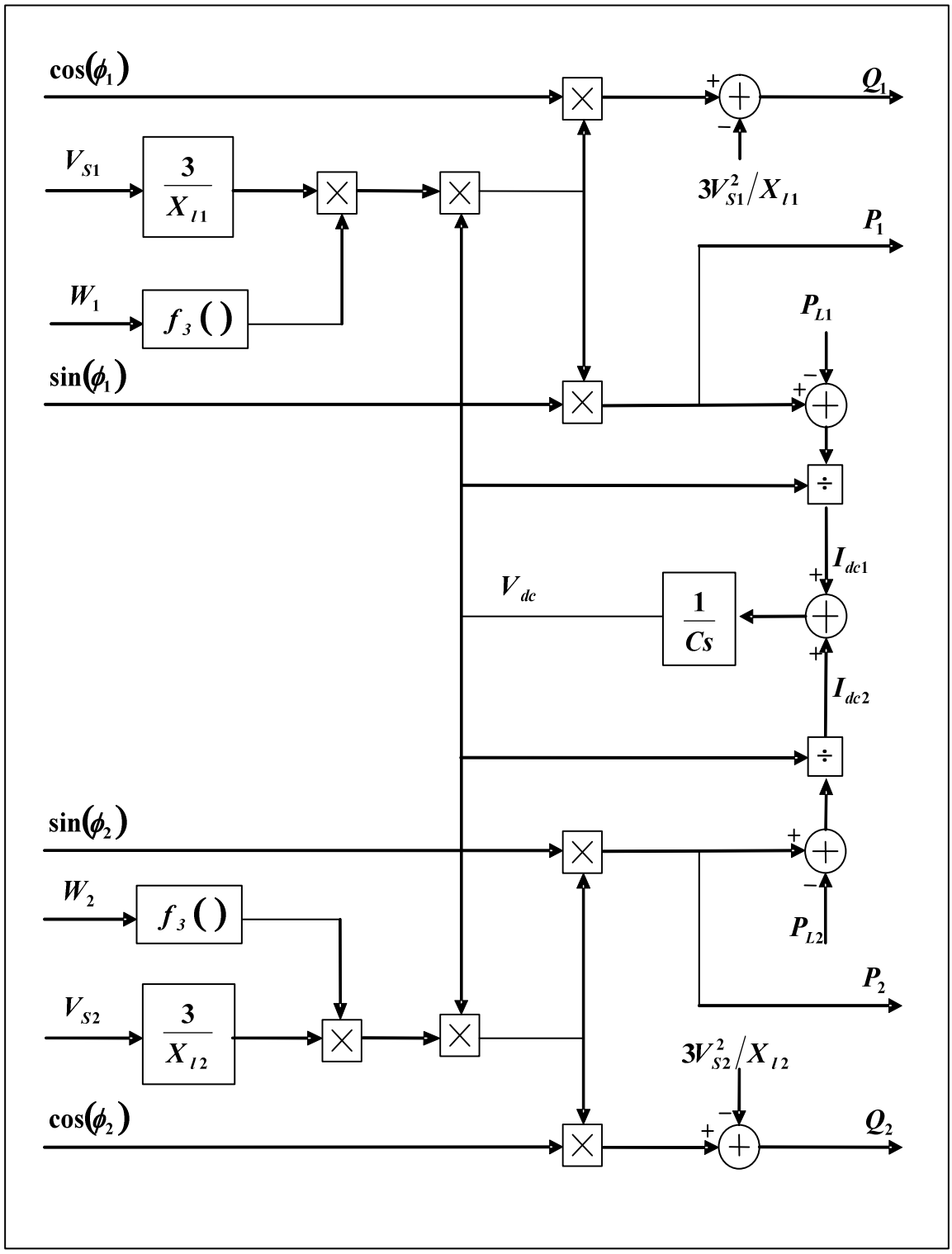


Figure 5.2 BTB-VSC link block diagram for control of active and reactive power.

be used as an approximation, with accuracy that increases as the step level number increases. Hence, V_{A1} and V_{A2} are simplified as

$$V_{A1} = V_{dc} \times f_3(W_1) \tag{5.2.1.5}$$

$$V_{A2} = V_{dc} \times f_3(W_2) \tag{5.2.1.6}$$

Based on equations 5.2.1.1-5.2.1.4, figure 5.2 shows the block diagram of the BTB-VSC link used for the control of active and reactive power.

5.2.2 Operation Region of the Back-to-back MLVR-VSC

MLVR-VSC provides high efficient commutation between the main bridge switches by means of ZVS condition which is obtained by varying the dc voltage levels across the main bridges. This desire for zero voltage commutations imposes a limitation on the output voltage fundamental component amplitude control. By introducing modulation notches on the dc side voltage waveforms, as discussed in chapter 4, limited amplitude control of the fundamental component is achievable.

In the model of figure 5.1, the topological structures of the two MLVR-VSCs are the same and they are tied to the same dc side voltage, V_{dc}. The fundamental voltage amplitude function is as expressed in equations 5.2.1.5 and 5.2.1.6. Usually the variation range of $f_3(W)$ is limited to 10% corresponding to a nominal interface transformer leakage reactance of 10%, as discussed in chapter 3. For analysis simplicity, the two power systems in figure 5.1 are treated as equally rated and hence, the rated source voltages, converter currents and interface transformer leakage reactances are equal, i.e. $V_{SRated}=V_{S1Rated}=V_{S2Rated}$, $I_{Arated}=I_{A1Rated}=I_{A2Rated}$ and $X_{l1}=X_{l2}$.

Prevention from conductor overheating requires that the converter output currents must be equal to or less than their rated values, and therefore the voltage across the two reactors are $V_{x1}=I_{A1}X_{l1}\leq I_{Arated1}X_{l1}$ and $V_{x2}=I_{A2}X_{l1}\leq I_{Arated}X_{l2}$. This requirement in terms of the phasor diagram in figure 5.3(a) means that the phasor V_{x1} must be located in a circle centred at the end of phasor V_{A1} with radius of $I_{Arated}X_{l1}$. Also phasor V_{x2} must be located in the circle centred at the end of phasor V_{A2} with radius of $I_{Arated}X_{l2}$. With adjustment of the dc side voltage and output voltage fundamental component control via notching

modulation, the end of phasors V_{A1} and V_{A2} can lie anywhere along the straight line bounded the arcs of V_{Amax} and V_{Amin}. V_{Amax} and V_{Amin} represent the maximum (when W=0°) and minimum (when W=5°) achievable fundamental output voltage amplitudes for some specified V_{dc}. The possible locations for the end of phasors V_{S1} and V_{S2} are within the circles centred at the end of phasor V_{A1} and V_{A2} with a radius of $I_{Arated}X_{l1}$ and $I_{Arated}X_{l2}$ respectively. These safe operating margins are shown in figure 5.3(a) by dotted circles. The V_{Amax} and V_{Amin} arcs are drawn in dashed lines and they indicate the controllable regions of the BTB-VSC.

For steady-state operation, based on the safe current operation limits, the maximum absolute values of ϕ_1 and ϕ_2 can be derived directly from the phasor diagram, i.e.

$$\left[\sin|\phi_1|\right]_{\max} = \frac{I_{ARated}X_{l1}}{V_{S1}} = \frac{V_{SRated}}{V_{S1}}\frac{X_{l1}}{V_{SRated}/I_{ARated}} = \frac{V_{SRated}}{V_{S1}}\frac{X_{l1}}{Z_{Base}} \qquad (5.2.2.1)$$

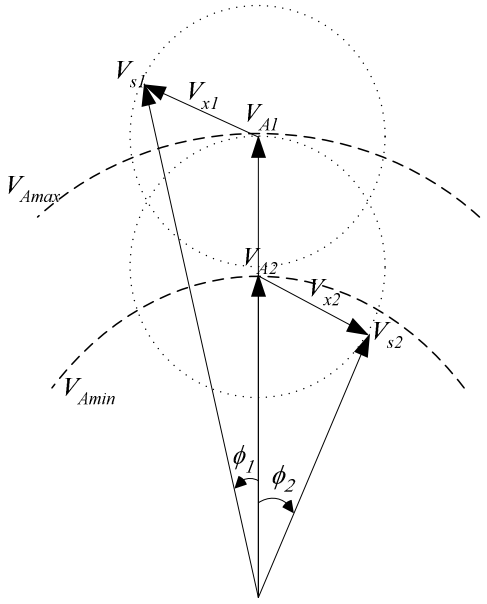
$$\left[\sin|\phi_2|\right]_{\max} = \frac{I_{ARated}X_{l2}}{V_{S2}} = \frac{V_{SRated}}{V_{S2}}\frac{X_{l2}}{V_{SRated}/I_{ARated}} = \frac{V_{SRated}}{V_{S2}}\frac{X_{l2}}{Z_{Base}} \qquad (5.2.2.2)$$

Assuming the system operates at rated voltages, i.e. V_{S1}=V_{S2}=V_{Srated}, equations 5.2.2.1-5.2.2.2 become

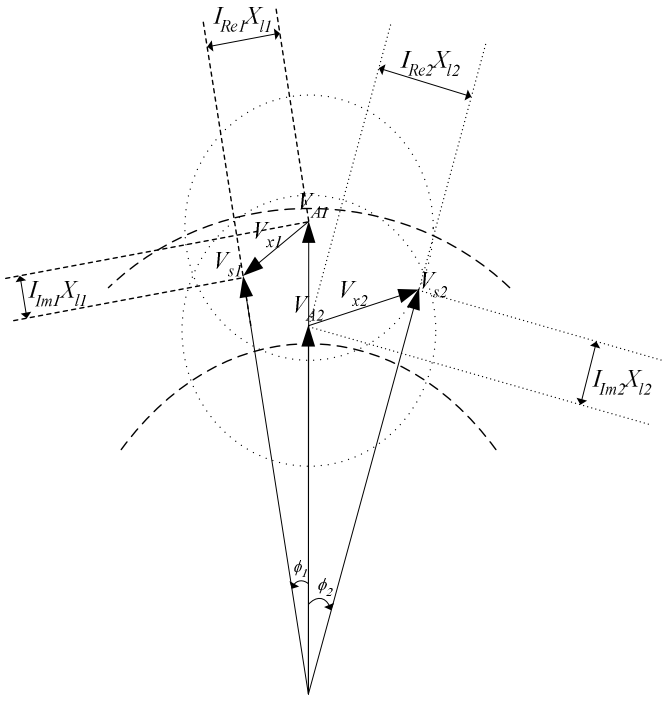
$$\left[\sin|\phi_1|\right]_{\max} = \frac{X_{l1}}{Z_{Base}} = x_{l1} \qquad (5.2.2.3)$$

$$\left[\sin|\phi_2|\right]_{\max} = \frac{X_{l2}}{Z_{Base}} = x_{l2} \qquad (5.2.2.4)$$

These equations imply that the interface transformer nominal leakage reactance X_l governs the possible operation region. For example, if the 60Hz source operates at rated condition, i.e. V_{S1}=V_{Srated}, the possible amplitude range of the converter output voltage, V_A, is from $V_{SRated}(1\text{-}x_l)$ to $V_{sRated}(1\text{+}x_l)$ and that of V_{S2} is from $V_{SRated}(1\text{-}3x_l)$ to $V_{sRated}(1\text{+}3x_l)$. Or in other words, under a $3x_l$ voltage depression the BTB-VSC link can operate safely, but the real power transfer and reactive power generation will be limited. Usually, the end of phasors V_{S1} and V_{S2} are kept within the part of the circles bounded by the V_{Amax} and V_{Amin} arcs so that the converters are able to perform compensation actions in respond to transients.



(a)



(b)

Figure 5.3 Phasor diagram of the BTB MLVR-VSC system
(a) Safe operation margin and reactive power controllability arc
(b) Steady state operation relationship between two converters

The losses in the dual converter system are neglected based on the assumption that the efficiency of MLVR-VSC is high. Thus the active power transferred from the two power systems to the dual converter system must be zero under steady-state condition. If both sides are operating at rated voltages, this restriction can be expressed by:

$$P_1 = P_2 = P \tag{5.2.2.5}$$

$$\frac{3V_{S1}V_{A1}}{X_{l1}}\sin(\phi_1) = \frac{3V_{S2}V_{A2}}{X_{l2}}\sin(\phi_2) \tag{5.2.2.6}$$

$$\frac{V_{A1}}{V_{A2}} = \frac{\sin(\phi_2)}{\sin(\phi_1)} \tag{5.2.2.7}$$

These equations predict that for some active power transfer through the link, the ratios between the converter fundamental voltage amplitudes and the inverse ratios between the sines of phase angle differences are equal, i.e. if the fundamental voltage amplitude on one side is increased to generate more reactive power, the phase angle difference on the other side has to be decreased accordingly in order to maintain real power balance.

The phasor diagram in figure 5.3(b) shows the steady-state operation restrictions under specified active power transfer. The circle centred at the end of phasor V_{A1} with radius of $I_{Arated}X_{l1}$ is the area of the end of phasor V_{S1} for safe operation; the circle centred at the end of phasor V_{A2} with radius $I_{Arated}X_{l2}$ is the area of the end of phasor V_{S2}. These circles can be divided into four equal-area quadrants along the V_A lines and the tangents of the end of V_A phasors. The left half indicates a supply of real power from the power system into the converter and the right half indicates a supply of real power from the converter into the power system. The upper and lower half regions indicate reactive power absorption and generation by the converter. Figure 5.3 shows that the amplitude of the two source voltages (V_{S1} and V_{S2}), the dc side voltage together with modulation notches width ($V_A = V_{dc} \times f_3(W)$), and the two controllable phase angles (ϕ_1 and ϕ_2) determine the dual system operating state and the interface transformer leakage reactances determine the possible safe operating region.

5.3 The Control Structure of the Back-to-back MLVR-VSC Link

5.3.1 Synchronisation Technique

The phase synchronisation function defined in PSCAD-EMTDC is used in this thesis. It is based on the phase vector technique [32], where the three phase commutation voltages V_A, V_B and V_C are transformed into dual-axis voltages, V_α and V_β, using

$$V_\alpha = \left(\frac{2}{3}\right)V_A - \left(\frac{1}{3}\right)V_B - \left(\frac{1}{3}\right)V_C \qquad (5.3.1.1)$$

$$V_\beta = \left(\frac{1}{\sqrt{3}}\right)(V_b - V_C) \qquad (5.3.1.2)$$

respectively. An error signal, V_{error}, derived using

$$V_{error} = V_\alpha V \sin\theta + V_\beta V \cos\theta \qquad (5.3.1.3)$$

is fed through a PI controller to generate a reference value for the voltage controlled oscillator (VCO). An offset, which is usually the ac system nominal frequency, is added to the reference value in order to maintain the VCO operation at nominal frequency when the ac commutation signals are lost due to transients and faults. The block diagram in figure 5.4 shows the phase-locked-oscillator (PLO) with its VCO being replaced by an integrator block without any phase delay. The output of the integrator is a resetable (every 2π) ramp signal. This output is fed to a sine-cosine generator. The sine-cosine waveforms are then fed back to the multipliers to generate the error signal. The sine waveform is also the synchronisation signal for the subsequent zero crossing detector.

5.3.2 Converter Switches Firing Logic

The synchronisation signal, obtained from the PLO is passed through the zero-crossing detector to provide the starting point for the ramp signal generator. 12 equally time-

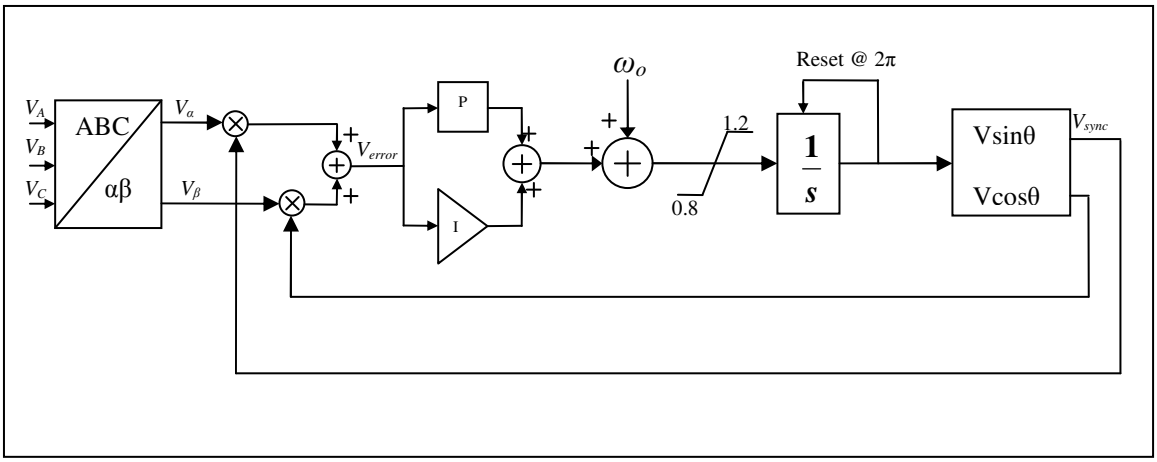


Figure 5.4 Block diagram of the phase-locked-oscillator (PLO).

spaced, at the interval of 30°, ramp signals are generated corresponding to 12 main bridge switches. The ramp signals for time-distance of 0°, 60°, 120°, 180°, 240° and 300° are grouped as *thetaY* while the 30°, 90°, 150°, 210°, 270° and 330° time-distant ramp signals are grouped as *thetaD*. ThetaY is used in the firing logic for Y/Y main bridge switches while thetaD is used in the firing logic for Y/Δ main bridge switches.

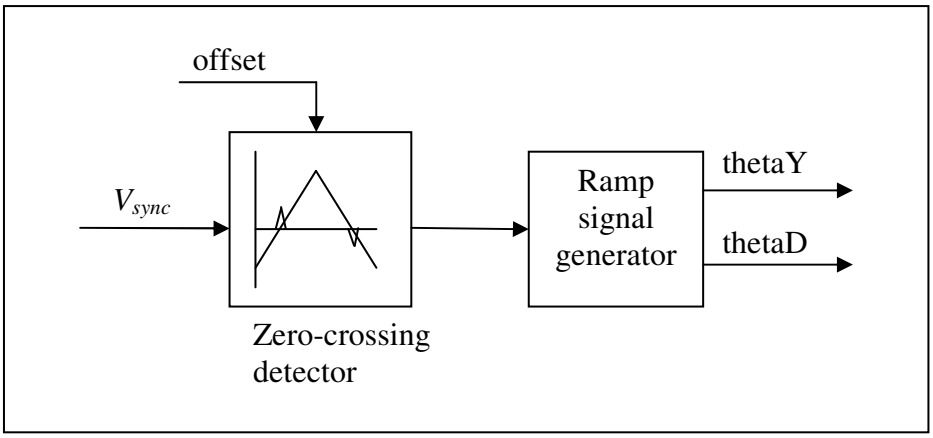


Figure 5.5 Block diagram of ramp signals generator.

As shown in figure 4.3, the switching frequency in the main bridges is three times per fundamental period. Thus, there are six comparators in each main bridge switch firing logic circuit, i.e. a group of three corresponds to switching on and another group of three corresponds to switching off. The comparison input signals for switch-on logic generation are $\phi_{order} - W_{order}/2$, $\phi_{order} - W_{order}/2$ and $\phi_{order} - (W_{order}/2 + e)$ (e is the bypass period required for voltage sharing mechanism between the H-bridge capacitor and dc main capacitors) while the comparison input signals for switch-off logic generation are

$\phi_{order} - W_{order}/2$, $\phi_{order} + W_{order}/2$ and $\phi_{order} + W_{order}/2$. These signals are compared against the ramp signals (thetaY and thetaD) in order to determine the switching instances of each switches. The comparisons are grouped as follow:

- In order to turn-on
  - S_{Y1}, $\phi_{order} - W_{order}/2$ is compared against thetaY(1) and thetaY(3) and $\phi_{order} - (W_{order}/2 + e)$ is compared against thetaY(6);
  - S_{Y2}, $\phi_{order} - W_{order}/2$ is compared against thetaY(2) and thetaY(4) and $\phi_{order} - (W_{order}/2 + e)$ is compared against thetaY(1);
  - $S_{\Delta 1}$, $\phi_{order} - W_{order}/2$ is compared against thetaD(1) and thetaD(3) and $\phi_{order} - (W_{order}/2 + e)$ is compared against thetaD(6);
  - $S_{\Delta 2}$, $\phi_{order} - W_{order}/2$ is compared against thetaD(2) and thetaD(4) and $\phi_{order} - (W_{order}/2 + e)$ is compared against thetaD(1); etc.

- And in order to turn-off
  - S_{Y1}, $\phi_{order} - W_{order}/2$ is compared against thetaY(3), $\phi_{order} + W_{order}/2$ is compared against thetaY(4) and thetaY(6);
  - S_{Y2}, $\phi_{order} - W_{order}/2$ is compared against thetaY(4), $\phi_{order} + W_{order}/2$ is compared against thetaY(5) and thetaY(1);
  - $S_{\Delta 1}$, $\phi_{order} - W_{order}/2$ is compared against thetaD(3), $\phi_{order} + W_{order}/2$ is compared against thetaD(4) and thetaD(6);
  - $S_{\Delta 2}$, $\phi_{order} - W_{order}/2$ is compared against thetaD(4), $\phi_{order} + W_{order}/2$ is compared against thetaD(5) and thetaD(1); etc.

The outcomes of the comparators in a group are summed together before they are fed to the inputs of a latch. Figure 5.6 shows the firing logic for switch S_{Y1}.

The ramp signal generator and firing logic block diagrams shown in figure 5.5 and figure 5.6 contain an offset input signal. This offset is used to provide the phase-shift necessary to compensate for negative values of the comparison input signals. This compensation is necessary because the ramp signals, thetaY and thetaD, only range from 0 to 2π. Negative values of comparison input signals will not provide any crossings with the ramp signals, which will cause the comparator malfunction.

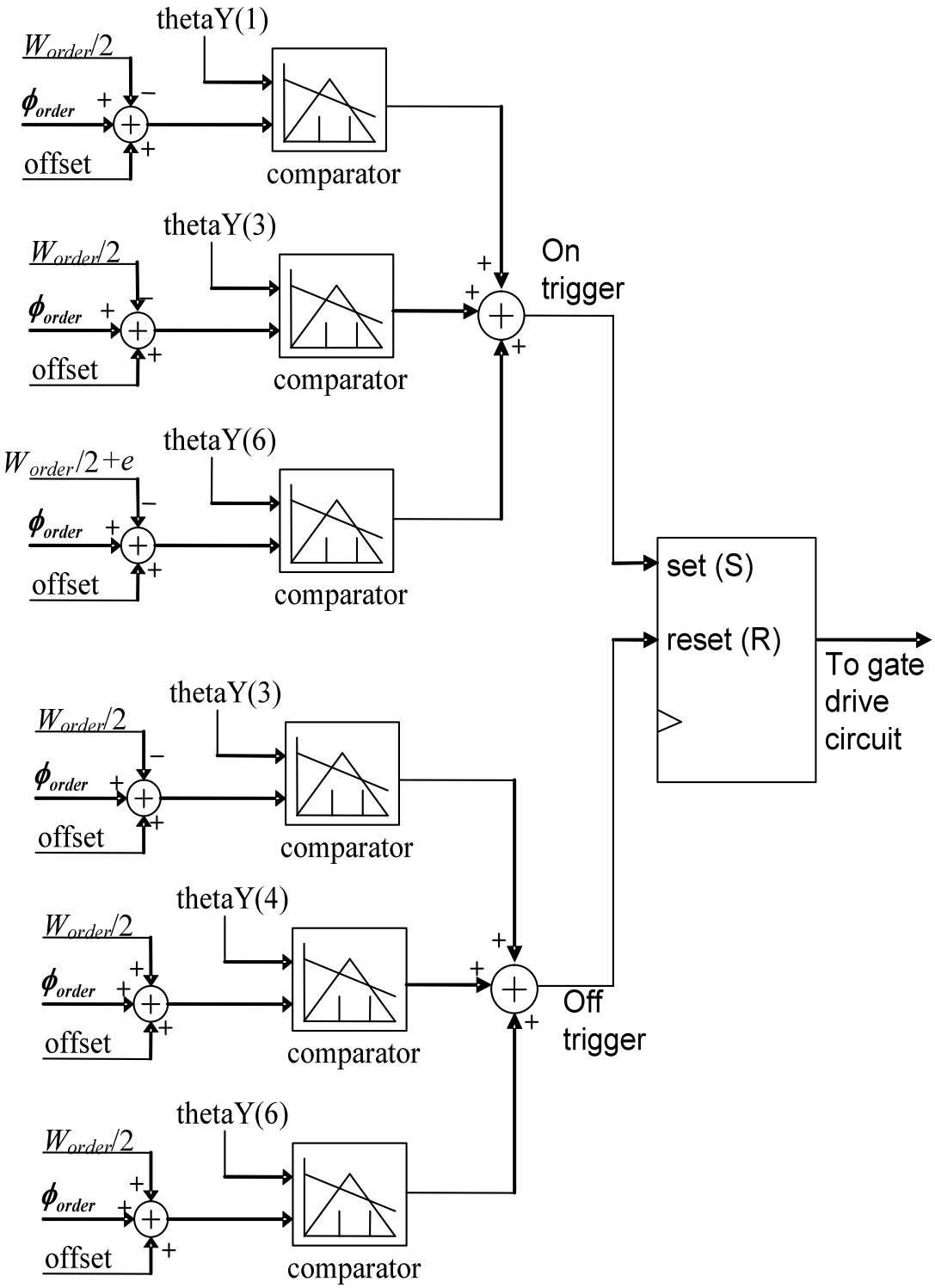


Figure 5.6 Firing logic for S_{Y1}.

5.3.3 Overall Control Loop

The transfer of specified real power and the independent generation of the required reactive power is the main goal of the BTB-VSC link control system. The active power transfer of one side is negatively related to that of the other side while the reactive power generation on both sides are independent (with some limitation). The dc bus voltage can be varied with some extend of freedom from the active power transfer and the reactive power generations. The purpose of controlling dc bus voltage is to optimise the converters operating conditions so that they can respond well to transients by determining the range of reactive power generation on both sides. Therefore, one active power transfer, two reactive power generations and one dc bus reference voltage are set as the command parameters.

The MLVR-VSC on each side is controlled via two separate control loops. One control loop corresponds to active power transfer control and the other corresponds to reactive power generation control. Because the active power transfer is more dependent on the phase angle difference between the power system source voltage and MLVR-VSC ac output voltage, active power transfer is controlled via the phase angle difference, ϕ. The reactive power generation control is controlled via the MLVR-VSC fundamental voltage amplitude control, which is achieved by varying the modulation notch widths (W). As explained earlier, this type of fundamental voltage amplitude control has limited range determined by the dc bus voltage. Therefore, the dc bus voltage has to be a compromise chosen by comparing the two power system characteristics. Dc bus voltage is controlled by the phase angle difference, which in turn controls the active power transfer to charge or discharge the dc main capacitors.

The four control loops (two for each side MLVR-VSC) shown in figure 5.7 consists of five PI controllers. The parameters denoted with subscript m, i.e. P_{m1}, Q_{m1}, P_{m2}, Q_{m2} and V_{dcm} are the measured parameters of the BTB-VSC link. The reactive power generation control loops for each MLVR-VSC are identical and they have one PI controller each. The output of these control loops are the modulation notch widths for each converter. The active power transfer control loops are also similar except that one side's active power controller is cascaded with the dc bus voltage controller. Each active power transfer control loop compares the measured active power flow, P_m, against the desired active

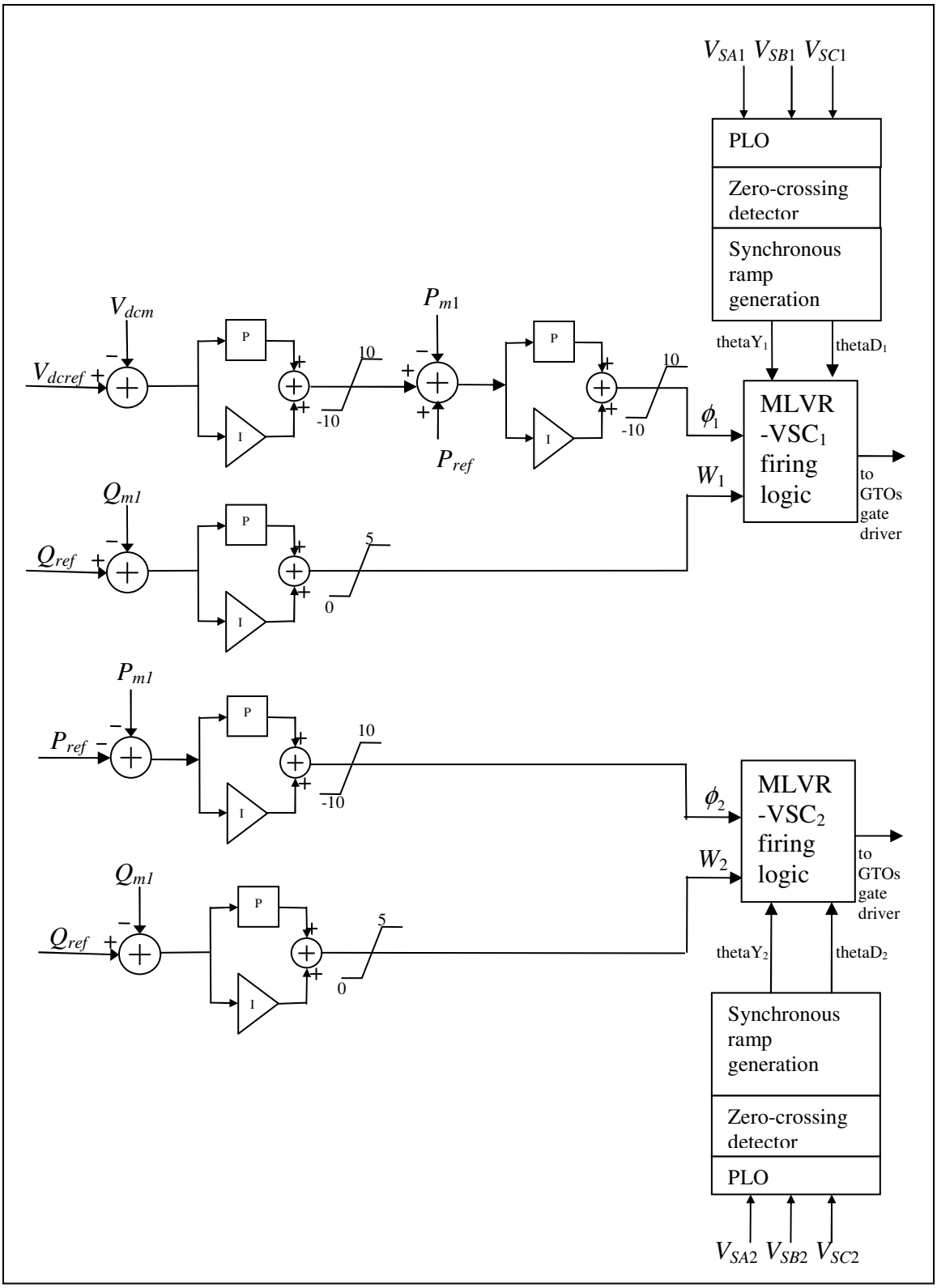


Figure 5.7 The BTB-VSC Link overall control loop.

power transfer, P_{ref}, and performs the corrective action to output the necessary phase angle difference. The dc bus voltage PI controller compares the measured dc bus voltage against the dc bus voltage set point. If they are not equal, the PI controller outputs the required active power, to charge or discharge the dc main capacitors, to be added to one side active power control loop. The reason for having only one side MLVR-VSC adjusting the dc bus voltage is to avoid counteractions between the two side controllers, which may have different action speeds. Normally, the dc bus voltage control loop is cascaded to the side with the generally faster response. In this case, it is power system 1 which has a nominal frequency of 60Hz.

A set of phase angle difference, ϕ, and modulation notch width, W, are fed into the firing logics of each MLVR-VSC respectively. These firing logics also receive input ramp signals from the synchronous ramp generators. The outputs of the firing logics are the inputs to the GTOs' gate drive circuits.

5.4 Test System and Simulation Results

5.4.1 PSCAD Simulation Package

The MLVR-VSC theoretical waveforms are verified by the EMTDC/PSCAD simulation package, which is an electromagnetic transient (EMT) studies tool based on Dommel's method [32]. EMTDC/PSCAD offers high performance in the simulation studies of power systems with power electronic devices. It has the enhanced abilities of time step interpolation and chatter removal algorithms which greatly improve the simulation studies accuracy.

5.4.2 MLVR-VSC Waveform Verification

A stand-alone MLVR-VSC was modelled, shown in figure 5.8, in the simulation package in order to verify the theoretical waveforms deduced in chapter 3. The model shown is a voltage source converter rated at 100MVA (i.e. two 50MVA 6-pulse bridges) and 100kV line-to-line voltage. The nominal leakage reactances of the interface transformers are 10%. A single H-bridge is used on the reinjection branch with a dc capacitor of 100μF.

The two main dc capacitors are 400μF each and the spike limiting inductor residing on the reinjection branch is 200μH. The source, which the converter is connected to, is modelled as ideal three phase voltage source, V_S, in series with internal impedances of 1Ω (80° phase lag). In order to allow the converter to transfer active power between the ac and dc bus, a variable dc source and resistor is added across the dc bus for this stand-alone model.

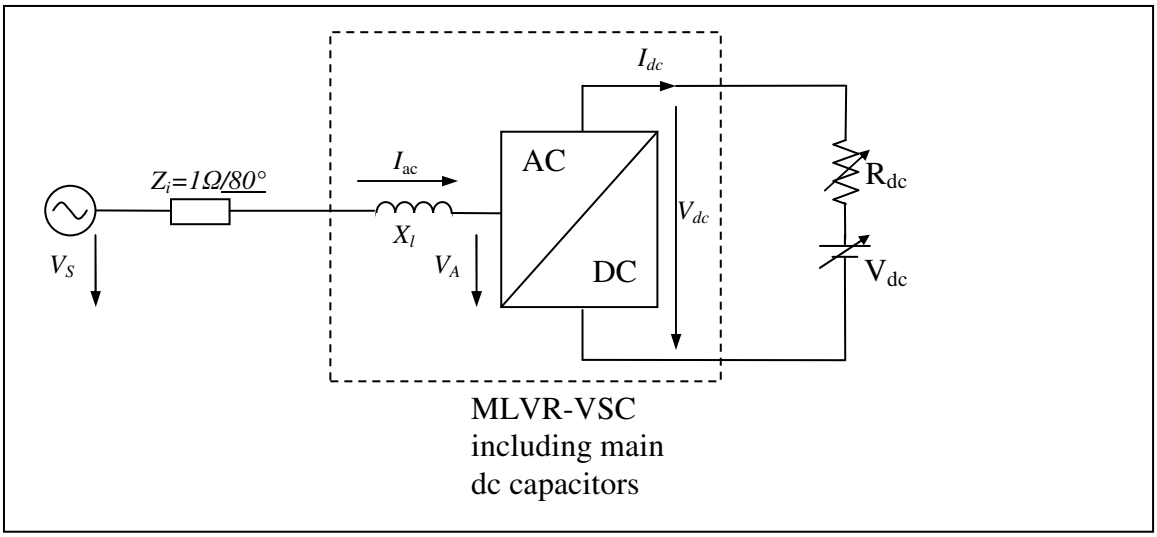


Figure 5.8 MLVR-VSC stand-alone model.

5.4.2.1 AC Side Output Voltage and Current

The stand-alone MLVR-VSC is simulated for rectifying operation at rated power for the purpose of presenting ac output waveforms with θ=0°. In figure 5.9, three cases of phase A line-to-ground converter output voltage are shown. They are the simulation results for modulation notch widths of 5° (full modulation), 2.5° and 0° respectively. The corresponding harmonics spectral for the ac output voltages are shown below each voltage waveforms. In figure 5.10, the converter ac output currents corresponding to the three widths of modulation notches are shown. The corresponding spectral analysis of the current harmonics are shown below each current waveforms.

Comparing the simulated V_A with the analytical output ac voltage V_A in chapter 4 (figure 5.9(a) to figure 4.5(f) and figure 5.9(e) to figure 4.2(f)), practically there is no difference in their shapes although the simulated voltages are plotted in true values. Table 5.1 lists

the voltage THDs for simulated waveforms against the theoretical ideal waveforms, based on equation 3.3.1.5, while table 5.2 lists the current THDs for simulated waveforms against the theoretical ideal waveforms, based on equation 3.3.2.10, for three values of *W*.

Table 5.1 THD_V comparison between simulated and ideal theoretical waveforms.

$THD_V(\%)$ \ W	0°	2.5°	5°
Simulated waveforms	7.75	15.4	21.22
Ideal theoretical waveforms	1.05	14.15	20.05

Table 5.2 THD_I comparison between simulated and ideal theoretical waveforms.

$THD_I(\%)$ \ W	0°	2.5°	5°
Simulated waveforms	2.87	5	10.33
Ideal theoretical waveforms	0.88	5.29	10.64

Finite step numbers appearing on the voltage waveforms causes the simulated output voltage THDs to be higher than the ideal theoretical values. In the simulation model, the MLVR-VSC is constructed using single H-bridge and hence the pulse number appearing on the ac output voltage is 24. Uncharacteristic harmonics caused by the capacitor voltage ripples also contribute to the increase in voltage harmonic content. For most of the simulated current THDs, they are lower than those derived in equation 3.3.2.10 because the slope of the modulation notches are finite in comparison to the modulation notches for ideal theoretical waveforms (which has vertical slope), the added internal impedance of V_s (which is mainly inductive) and the limited number of sample points, n_s, per cycle in the simulation. The last reason causes very high order ($h>n_s/2$) components to be discarded during the discrete FFT for analysing harmonic content.

The output voltage waveform shapes will remain relatively similar for any power angle, θ, and fixed modulation notch width, *W*, while the output current waveform shapes may differ for different power angles. This is because the phase-shifts of the harmonic components relative to the current fundamental component vary with different power angles. Current harmonic spectral, however, will be identical to those shown in figure 5.10 and hence the output current THDs, at rated power, should be the same for any power angles.

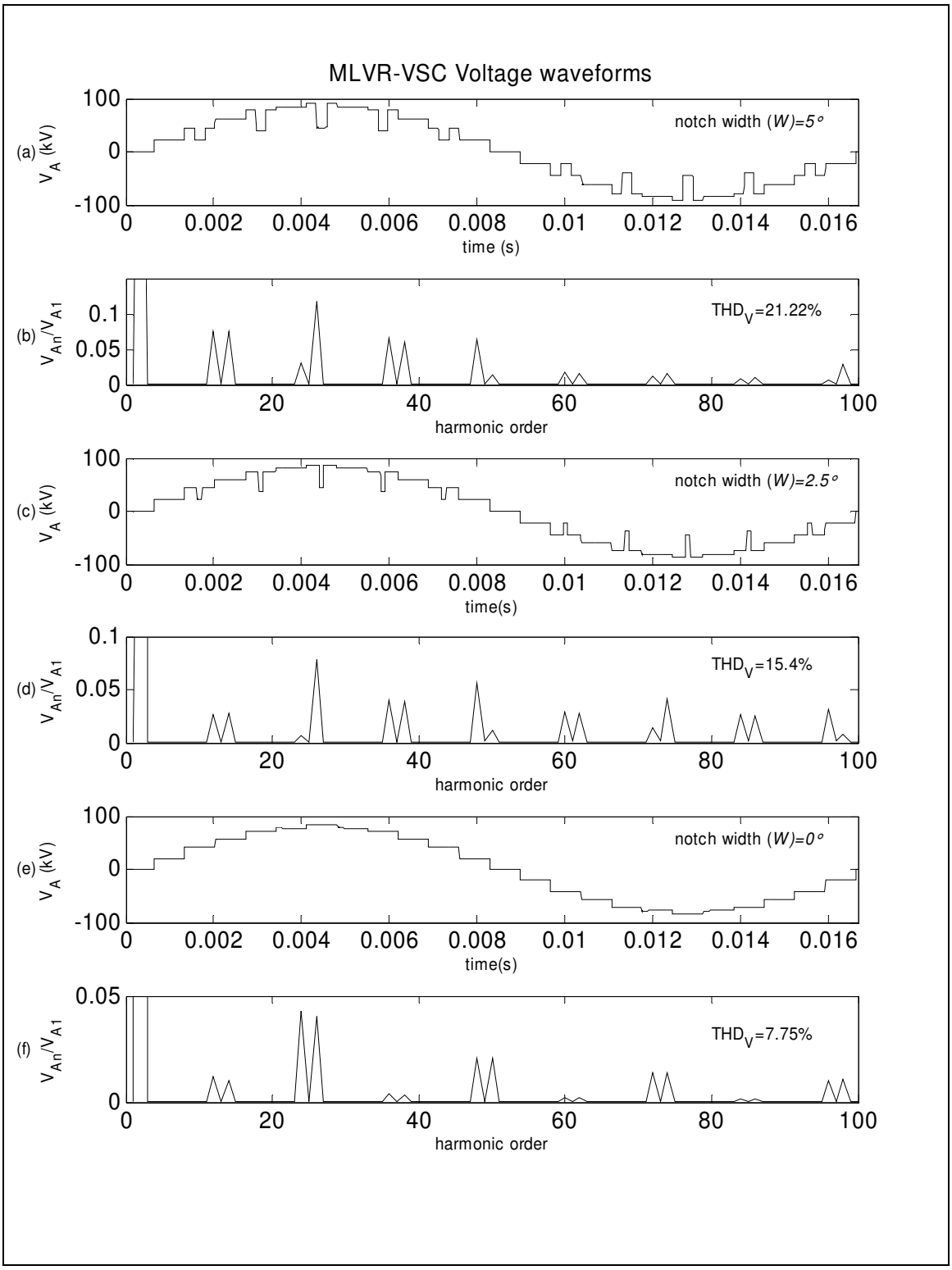


Figure 5.9 MLVR-VSC ac voltage waveforms and harmonics spectral.

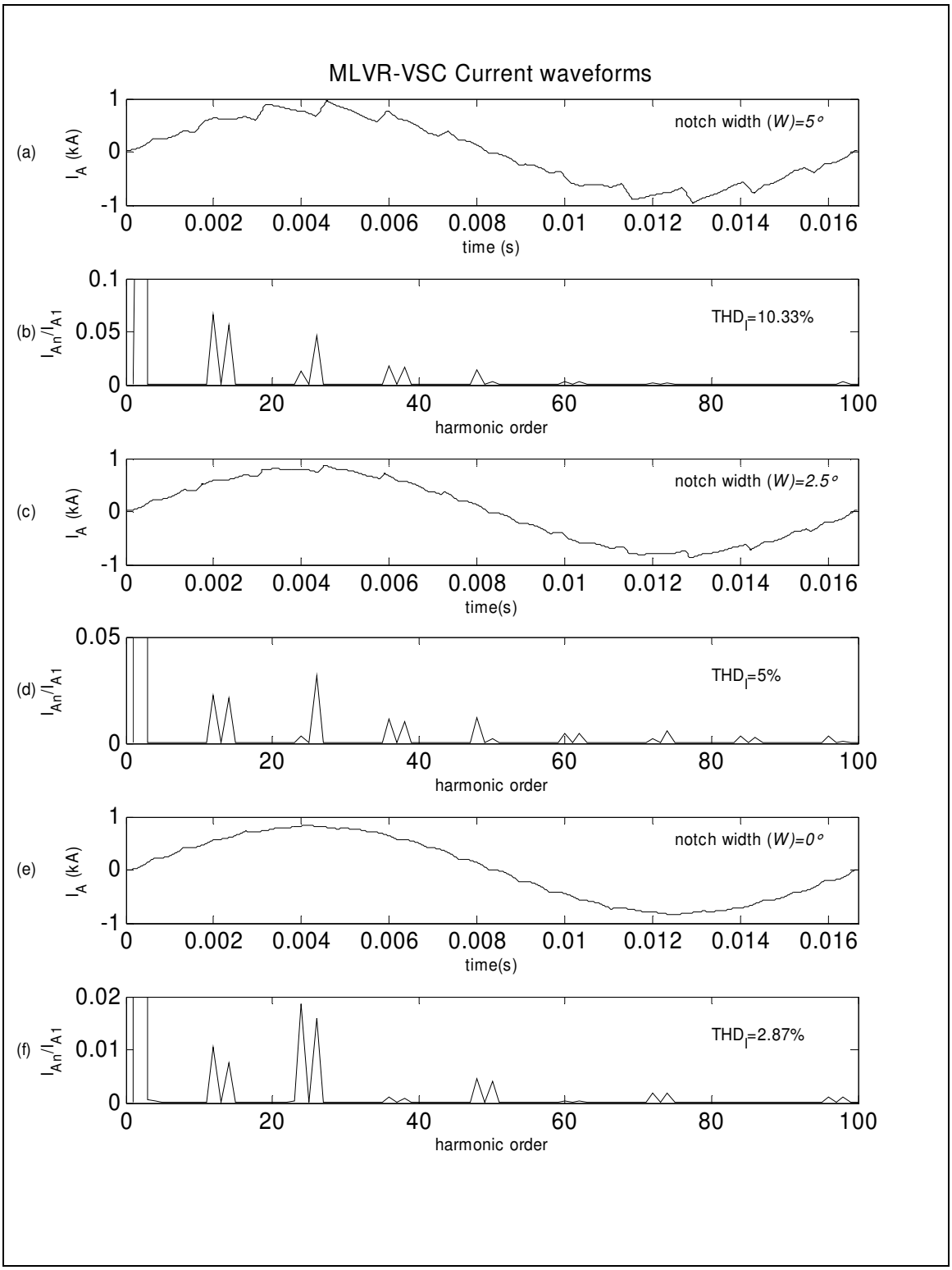


Figure 5.10 MLVR-VSC ac current waveforms and harmonics spectral.

5.4.2.2 DC Side Voltage and Current

Both inverting (θ=180°) and inductive (θ=90°) operation at rated power in the stand-alone MLVR-VSC model was simulated for the purpose of verifying the analytical dc side current paths deduced in chapter 4. The converter dc side waveforms, together with the main bridges switching functions, are shown in figure 5.11, for inverting operation, and figure 5.12, for inductive operation. The dc side waveforms for rectifying and capacitive operations are mirror images of those shown. The waveforms shown in figure 5.11 and 5.12 are:

(a) S_{y1}:S_{y6}, the switching functions of the switches on the Y/Y main bridge (amplitudes enlarged to various levels to show the time delay relationship);
(b) I_{Ydc}, the dc side current of the Y/Y main bridge;
(c) $S_{\Delta 1}$:$S_{\Delta 6}$, the switching functions of the switches on the Y/Δ main bridge (amplitudes enlarged to various levels to show the time delay relationship);
(d) $I_{\Delta dc}$, the dc side current of the Y/Δ main bridge;
(e) I_r, the reinjection branch current with reference direction as shown in figure 4.1.
(f) V_{Lr}, the voltage across the inductor residing on the reinjection branch with reference polarity as shown in figure 4.1.

The output voltage waveform modulation on the MLVR-VSC ac side is transformed into current modulation on the dc side. From figure 5.11 and 5.12, it can be seen that the I_{Ydc} and $I_{\Delta dc}$ are repetitive for every 60° and they are 30° phase-shifted from each other. The periods at which I_{Ydc} and $I_{\Delta dc}$ absolute values are zero coincide with the periods when the notches appear on the ac output voltage. During these periods, the main bridge dc side current paths are broken by either opening the upper arm valves ($S_{\Delta 1}$, $S_{\Delta 3}$ and $S_{\Delta 5}$ for Y/Δ main bridge; S_{Y1}, S_{Y3} and S_{Y5} for Y/Y main bridge) and closing lower arm valves ($S_{\Delta 2}$, $S_{\Delta 4}$ and $S_{\Delta 6}$ for Y/Δ main bridge; S_{Y2}, S_{Y4} and S_{Y6} for Y/Y main bridge) or opening the lower arm valves ($S_{\Delta 2}$, $S_{\Delta 4}$ and $S_{\Delta 6}$ for Y/Δ main bridge; S_{Y2}, S_{Y4} and S_{Y6} for Y/Y main bridge) and closing upper arm valves ($S_{\Delta 1}$, $S_{\Delta 3}$ and $S_{\Delta 5}$ for Y/Δ main bridge; S_{Y1}, S_{Y3} and S_{Y5} for Y/Y main bridge).

Because only one main bridge dc side current path is broken at any instant of notching (the dc side current path of one main bridge is broken alternately for every 30° while the other maintains conventional operation), the currents of the main bridge with unbroken dc side current path will be diverted to flow through the reinjection branch. This is

verified by the I_r waveforms shown in figure 5.11 and 5.12. Figure 5.11 is more obvious because there is a dc component involved in I_{Ydc} and $I_{\Delta dc}$ associated with active power transfer. High voltage stress is seen across the inductor on the reinjection branch for active power operation due to high di/dt of I_r associated with diversion of high main bridge current into the reinjection branch.

The alternate notching action of the Y/Δ and Y/Y main bridge and their current direction cause the diverted main bridge current to appear as alternating to the reinjection branch. Although the overall waveform shape of I_r is ac periodic over every 30° period, I_r can be rectified, during active power operation, into dc power to charge or discharge the H-bridge capacitor, depending on the switching functions of the H-bridge valves.

Figure 5.13 and 5.14 shows the simulated capacitor voltages and currents for inverting and inductive operations at rated power. The waveforms shown are:

(a) I_{C1}, the current into the dc main capacitor across Y/Δ main bridge terminal and the reinjection branch;
(b) I_{C2}, the current into the dc main capacitor across Y/Y main bridge terminal and the reinjection branch;
(c) I_{Cr}, the current into the H-bridge capacitor;
(d) V_{C1}, the voltage of the dc main capacitor across Y/Δ main bridge terminal and the reinjection branch;
(e) V_{C2}, the voltage of the dc main capacitor across Y/Y main bridge terminal and the reinjection branch;
(f) V_{Cr}, the voltage of the H-bridge capacitor.

In figure 5.13, the simulated capacitor voltage ripples are 0.7kV and 0.9kV (with 136.5kV dc bus voltage) for dc main capacitors and H-bridge capacitor respectively. In figure 5.14, the simulated capacitor voltage ripples are 0.5kV and 0.8kV (with 121kV dc bus voltage) for dc main capacitors and H-bridge capacitor respectively. Capacitor voltage ripples during active power operation are larger because the diverted main bridge currents from the dc main capacitors into the reinjection branch involve a dc component. Dc current is pushed into the dc main capacitor temporarily while the main bridge dc side current path is broken during the notching period. The voltage sharing mechanism during active power transfer also creates larger dynamics. The voltage drifts between H-bridge

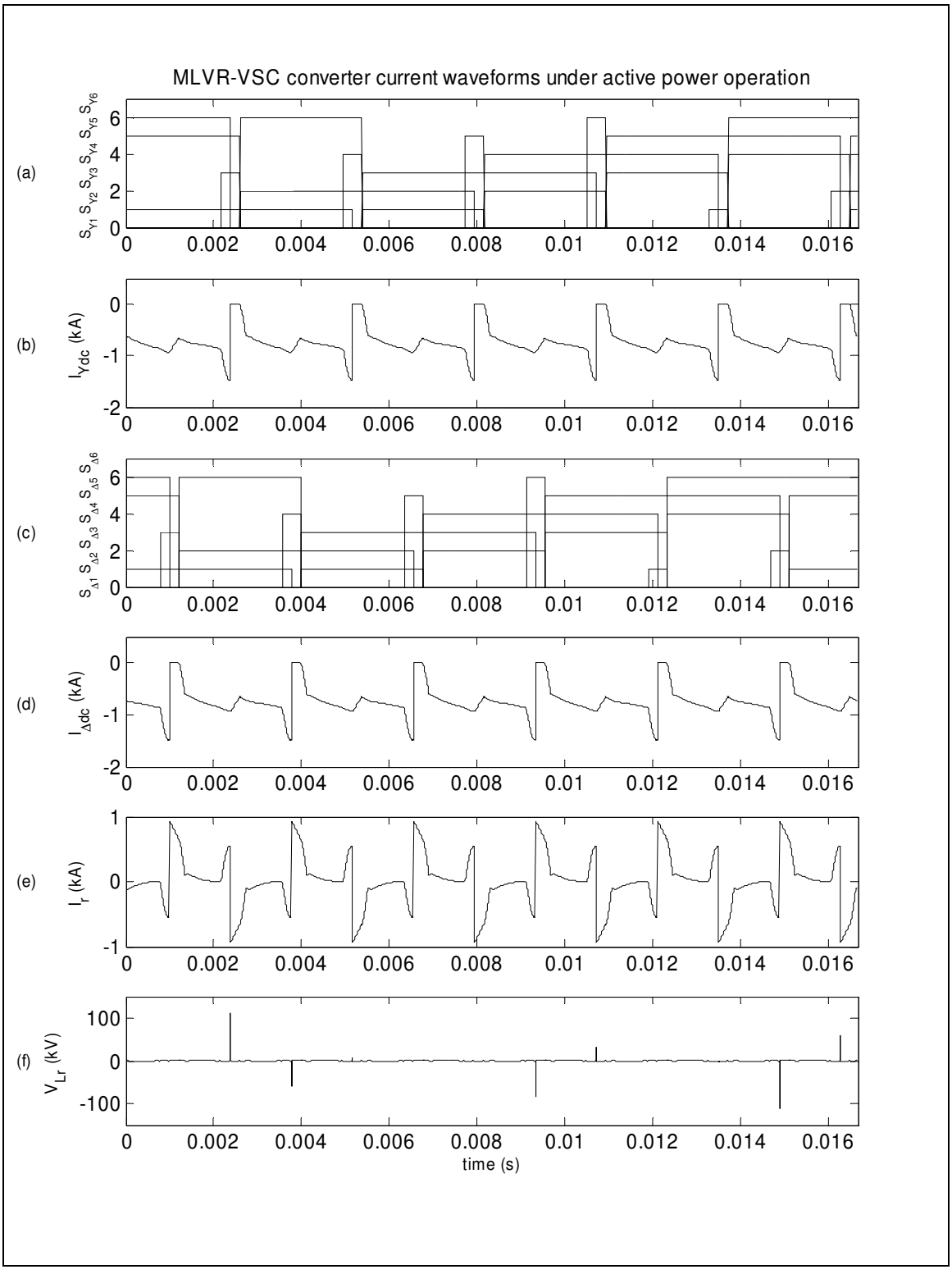


Figure 5.11 MLVR-VSC dc side current waveforms under inverting operation.

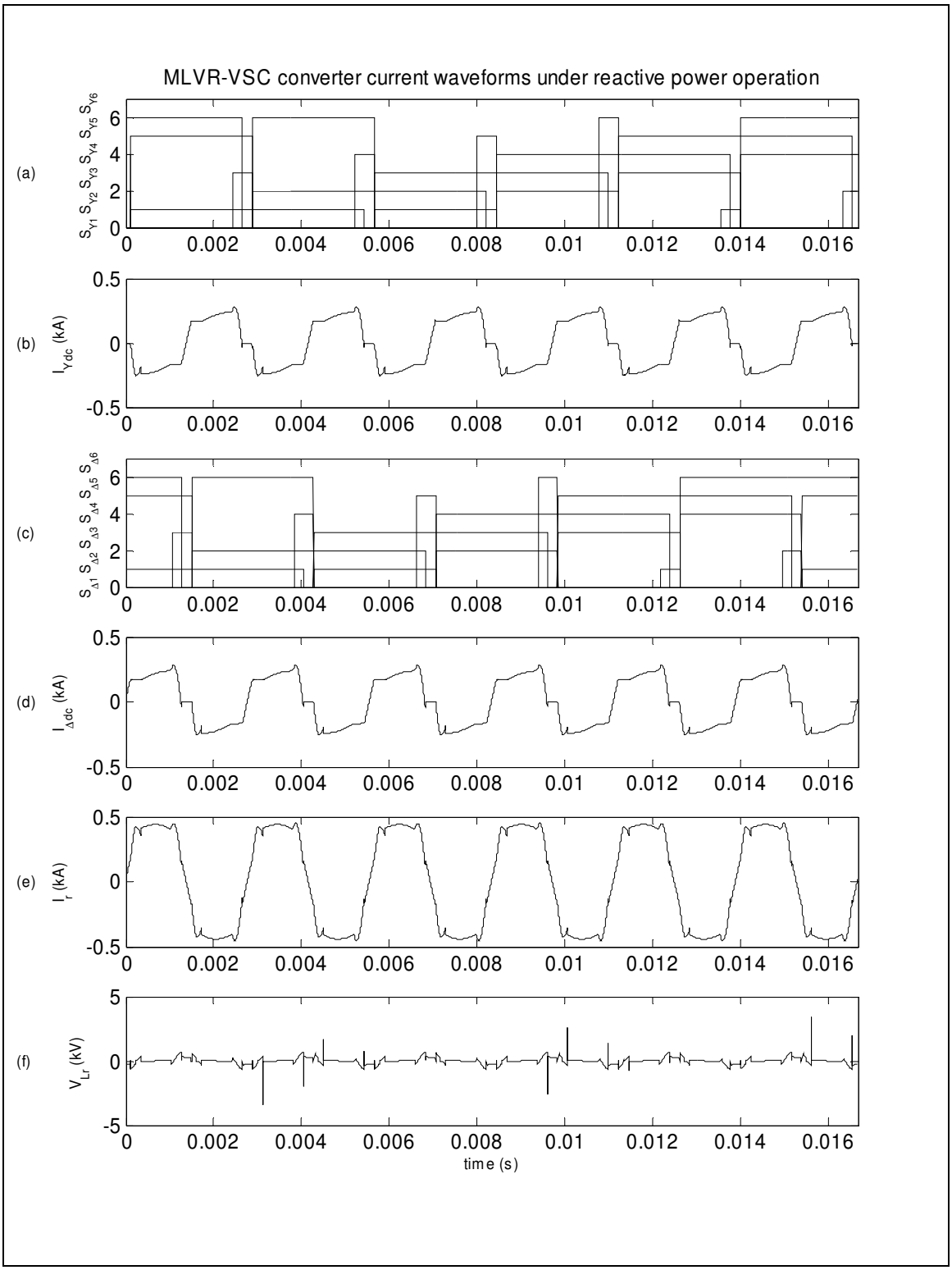


Figure 5.12 MLVR-VSC dc side current waveforms under inductive operation.

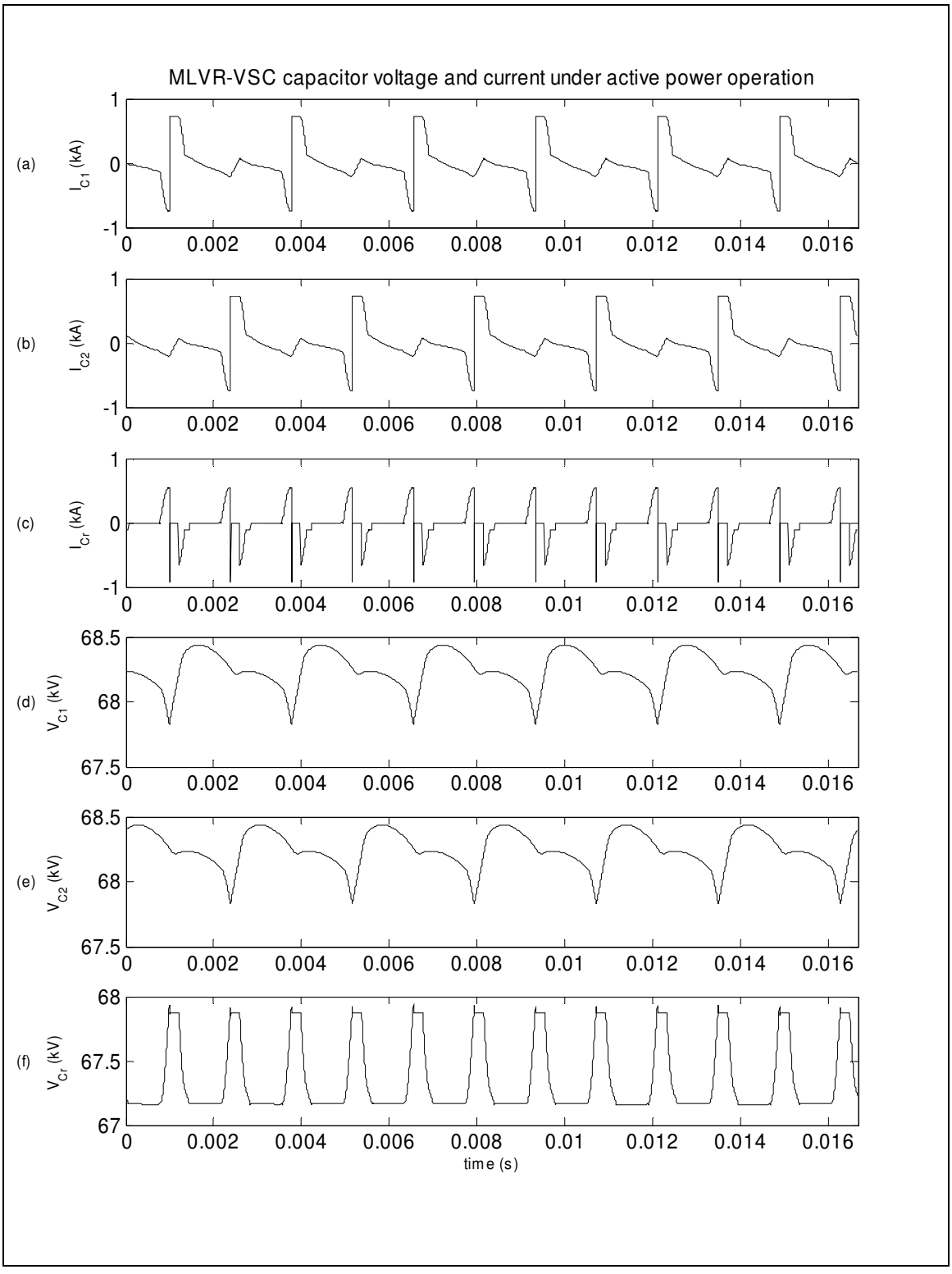


Figure 5.13 MLVR-VSC capacitor dynamics under inverting operation.

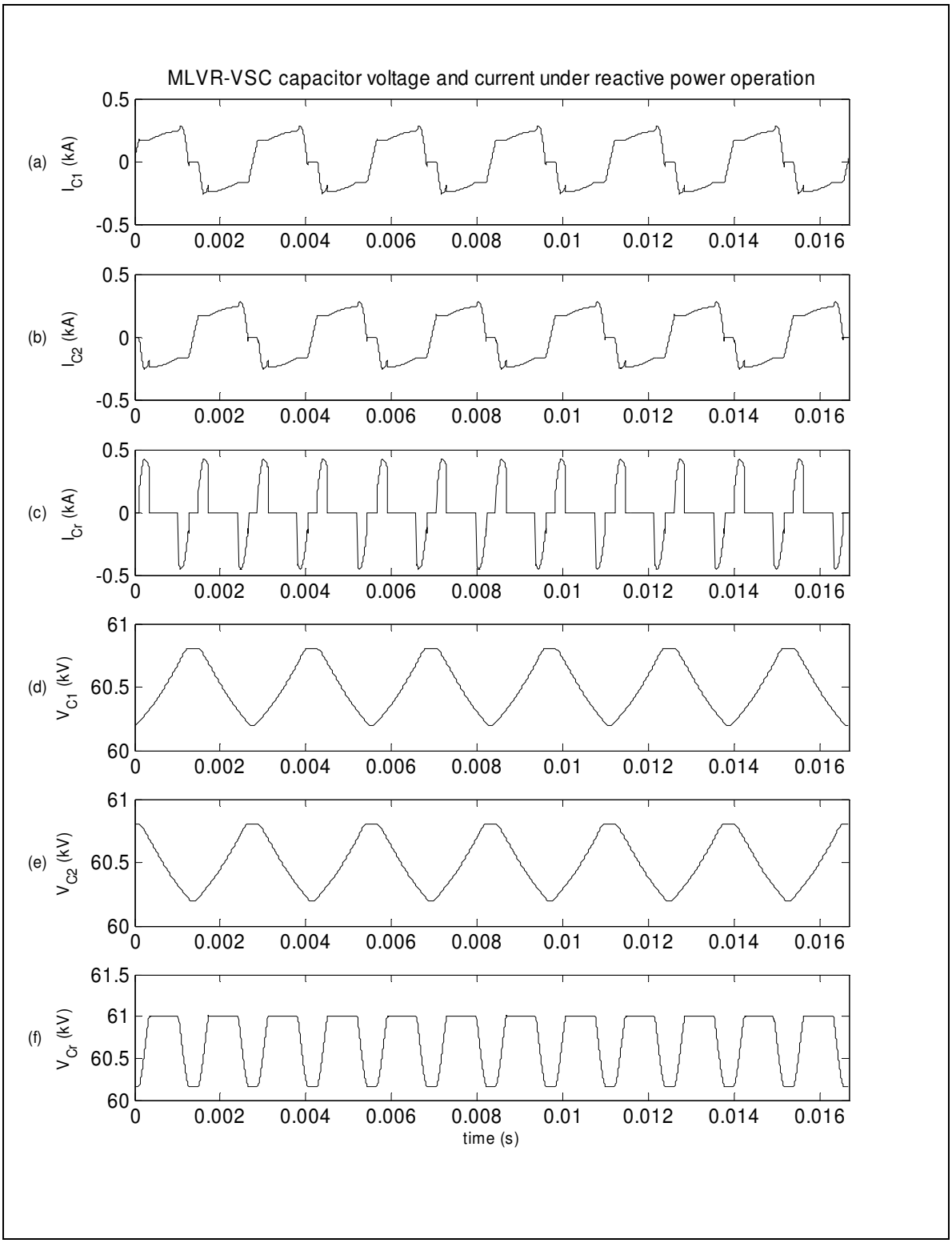


Figure 5.14 MLVR-VSC capacitor dynamics under inductive operation.

capacitor and dc main capacitors are larger due to the rectified I_r into dc power by the H-bridge valves switching functions.

The peaks seen on I_{Ydc} and $I_{\Delta dc}$ before the notching periods are the spike caused by the voltage sharing mechanism. During these periods, the main bridge valves are bypassed alternately to transfer charges between the H-bridge capacitor and alternate dc main capacitors. It can be seen that the I_{Ydc} and $I_{\Delta dc}$ spikes for the case of active power operation (1.4kA) are larger than those for the reactive power operation (0.3kA). This is due to the drift between the main dc capacitors and the H-bridge capacitor voltages ($|V_{C1}$-$V_{Cr}|$ or $|V_{C2}$-$V_{Cr}|$) prior to the bypass period is larger for active power operation.

The special conduction path mentioned in section 4.4.3 can be seen on I_{Ydc} and $I_{\Delta dc}$, after the notching period for the MLVR-VSC under reactive operation (figure 5.14). The anti-parallel diodes on the main bridges are forward biased alternately to allow charge transfer from H-bridge capacitor to alternate dc main capacitors. This conduction path is broken when V_{C1} or V_{C2} becomes higher than V_{Cr}.

5.4.3 BTB MLVR-VSC's Response to Transients

The effects of using the control loops depicted in figure 5.7 are investigated in the following four sections (5.4.3.1, 5.4.3.2, 5.4.3.3 and 5.4.3.4).

5.4.3.1 Active Power Response

Figure 5.15 and 5.16 show the BTB-VSC link dynamic response under normal conditions to step changes in the active power transfer with zero reactive power generations on both sides. Initially, the MLVR-VSC link operates with zero apparent power. After t=0.5s, the active power transfer control order is set to 100MW (1p.u.) from the 60Hz system to the 50Hz system under rated voltage condition. After t=1.45s, the order is reversed, and at t=3.4s the active power transfer order is set to zero again. The plots in figure 5.15 show the dynamic behaviour of the active and reactive powers of the two systems (P_{60}, Q_{60}, P_{50} and Q_{60}) and two phase angle displacements between the sources and the converter output voltages (ϕ_{60}, ϕ_{50}) in the period of 0<t<4s. The plots in figure 5.16 show the BTB-VSC link voltage and current waveforms, which are:

(a) V_{dc}, the dc bus voltage (across two main dc capacitors, C_1 and C_2);
(b) I_{dc60} and I_{dc50}, the dc side output currents of the 60Hz and 50Hz system side converters;
(c) V_{C1}, V_{C2} and V_{r60}, the voltages of the dc main capacitors across Y/ Δ and Y/Y main bridge respectively and 60Hz side MLVR-VSC H-bridge capacitor;
(d) V_{C1}, V_{C2} and V_{r50}, the voltages of the dc main capacitors across Y/ Δ and Y/Y main bridge respectively and 50Hz side MLVR-VSC H-bridge capacitor;
(e) V_{A60} and I_{A60}, the phase A output voltage and current of the 60Hz side MLVR-VSC;
(f) V_{A50} and I_{A50}, the phase A output voltage and current of the 50Hz side MLVR-VSC.

The plots in figure 5.15 show that it takes about 0.4s for the converters to reach 98% of the desired active power transfers. From the plotted active power response, the noticeable unsmooth nature of the active power's ascent and descent is due to the reaction from the V_{dc} controller. Due to the fact that both side MLVR-VSCs have a different response speed, the V_{dc} controller, which is cascaded to one side active power controller, is bound to affect the active power transfer change in order to maintain the dc bus voltage at some relatively constant value. The dc bus voltage dynamics caused by the active power transfer order step change is well controlled to a very small value (3kV for 132kV nominal dc bus voltage, i.e. $V_{dc_ripple}\approx 0.025$p.u.).

Waveforms of I_{dc60}, I_{dc50}, V_{C1}, V_{C2}, V_{r50}, V_{r60}, V_{A60}, I_{A60}, V_{A50} and I_{A50} are shown in greater detail in figure 5.16 for the interval of $2.4<t<2.6$s in order to show the dynamic process more clearly. Plots 5.16(c) and 5.16(d) show that all the capacitor voltages track well to each other but include some ripples. It should be noted that limited plotting steps have caused the discrepancies where the V_{r60} waveform do not intersect with V_{C1} and V_{C2} although this is not the case in true simulation results. The capacitor voltages highest ripple is seen on the V_{r60} waveform during which the 60Hz side MLVR-VSC is inverting 100MW active power and generating zero reactive power to the power system. The plots of ac output voltages and currents (V_{A60}, I_{A60}, V_{A50} and I_{A50}) show that the dynamics are well controlled with no over current. A notable fact is that the voltage waveforms remain relatively identical after the active power transfer order change while the harmonics on the current waveforms seem to have phase-shifted 180°. This confirms the analysis mentioned in section 5.4.2.1.

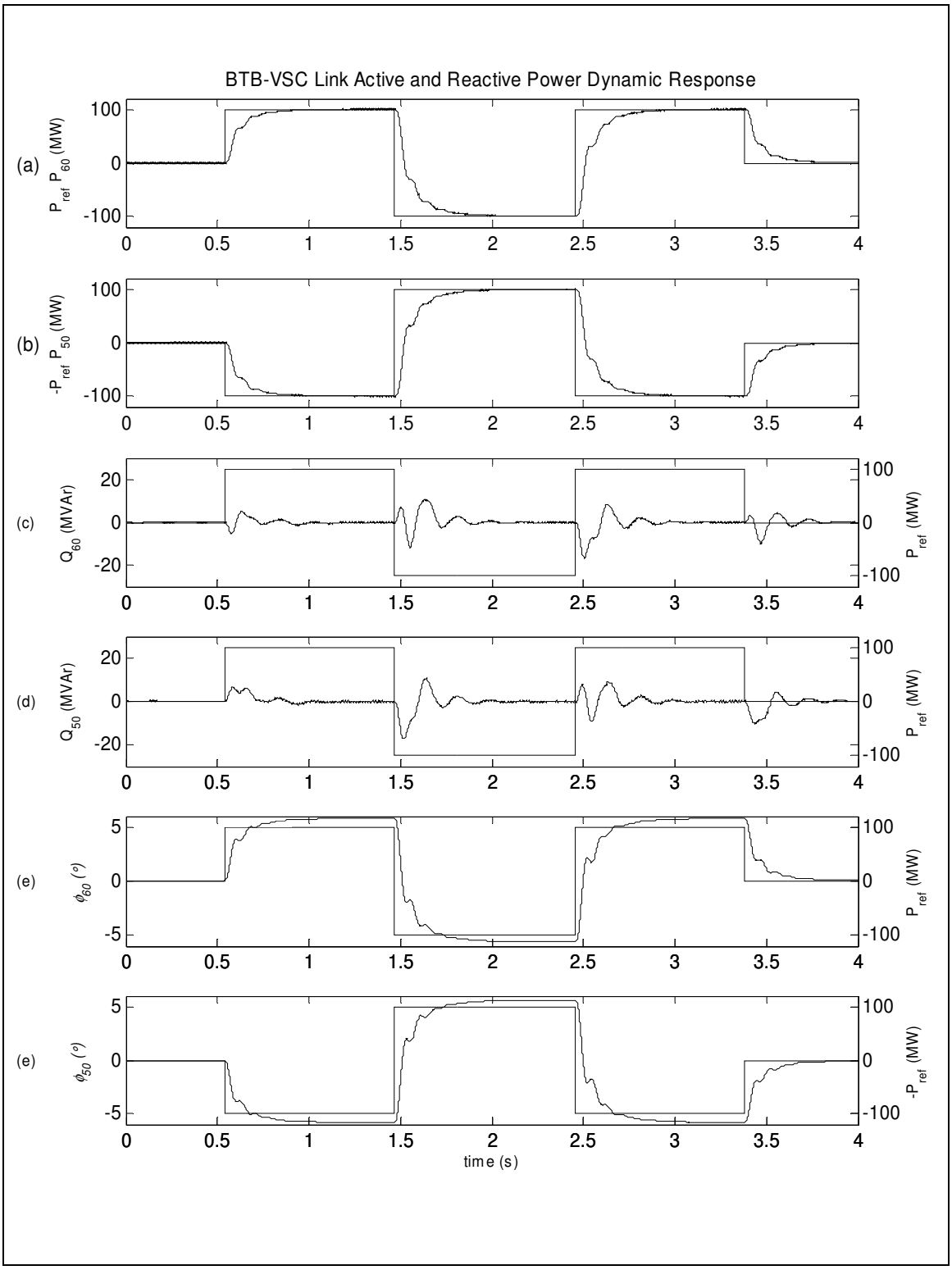


Figure 5.15 Active and reactive power response to active power order.

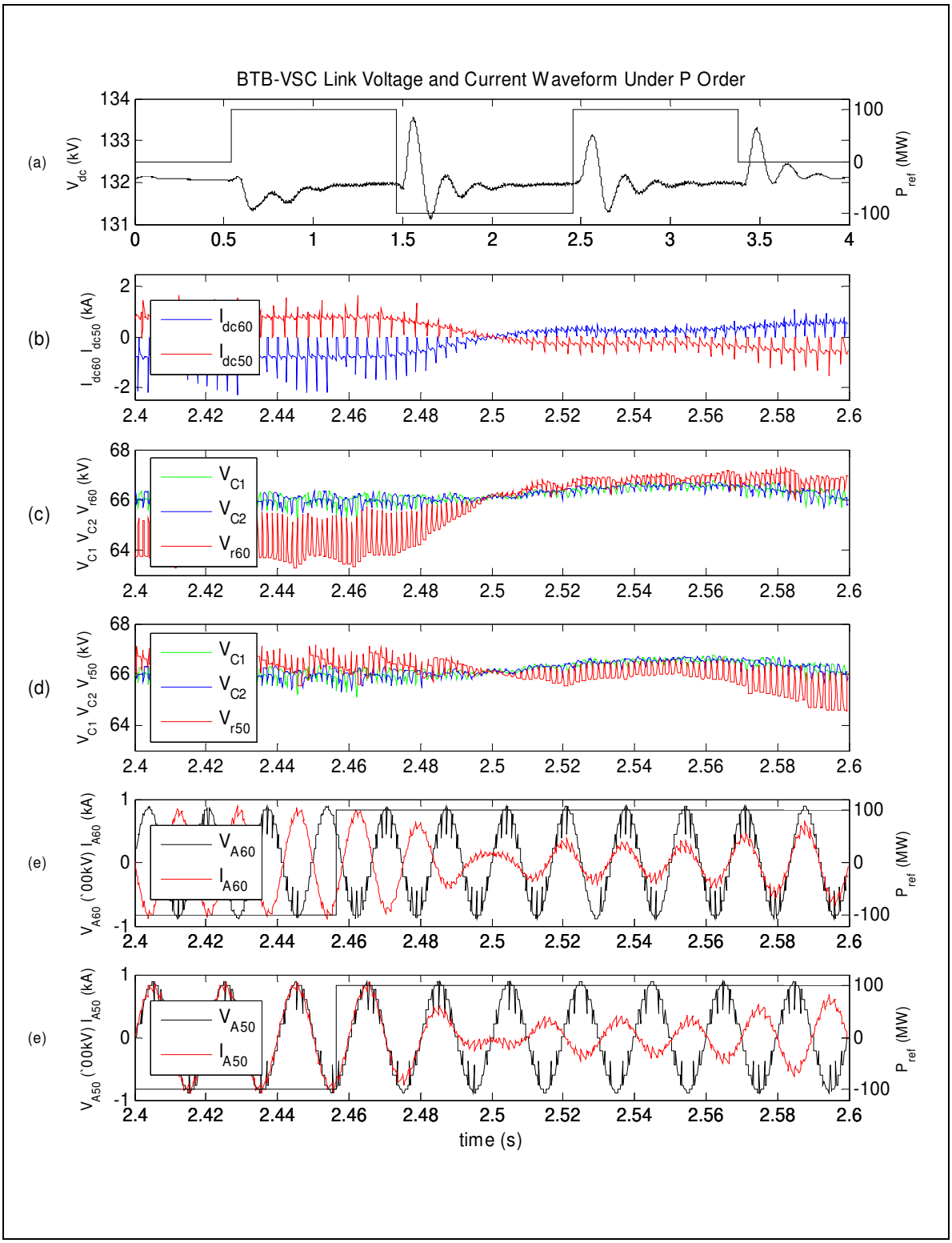


Figure 5.16 Voltage and current responses to active power order.

5.4.3.2 Reactive Power Response

Figure 5.17 and 5.18 show the BTB-VSC link dynamic response under normal conditions to independent step changes in both side's reactive power generation and zero active power transfer. Initially, the MLVR-VSC link operates with zero apparent power. After t=0.4s, the 60Hz side reactive power generation control order is set to 40MVAr (0.3p.u.) under rated voltage condition. After t=1.2s, the 50Hz side MLVR-VSC is ordered to generate 20MVAr reactive power to the power system. At t=2.05s, the 60Hz side MLVR-VSC is ordered to generate 40MVAr to the power system and 50Hz side MLVR-VSC is ordered to consume 40MVAr reactive power from the power system. After t=3s, the reactive power generation orders are set to zero again. The plots in figure 5.17 show the dynamic behaviour of the active and reactive powers of the two systems (P_{60}, Q_{60}, P_{50} and Q_{60}) and the modulation notches widths of each MLVR-VSC respectively (W_{60} and W_{50}) in the period of $0<t<4$s. The voltage and current waveforms in figure 5.18 are arranged as those in figure 5.16.

All the plots in figure 5.17 show that it takes about 0.4s for the converter to reach 98% of the desired reactive power generations. From the plotted reactive power response, it is noticeable that one side's reactive power generation change will cause transients on the other side's reactive power. The highest recorded interaction from simulation in figure 5.17 is 10MVAr. The reactive power responses of individual MLVR-VSC to independent reactive power generation order show a general damped second-order characteristics. However, at around t=2.05s, the simultaneous opposite actions of the two side MLVR-VSC has caused the reactive power response to show overdamp characteristics. The dc bus voltage dynamics caused by the reactive power generation orders step change is well controlled to very small value (1kV for 130.5kV nominal dc bus voltage).

Waveforms of I_{dc60}, I_{dc50}, V_{C1}, V_{C2}, V_{r50}, V_{r60}, V_{A60}, I_{A60}, V_{A50} and I_{A50} are shown in greater detail in figure 5.18 for the interval of $2.05<t<2.25$s in order to show the dynamic process more clearly. Plots 5.18(c) and 5.18(d) show that all the capacitor voltages track well to each other but contain some ripples. The plots of ac output voltages and currents (V_{A60}, I_{A60}, V_{A50} and I_{A50}) show that the dynamics are well controlled with no over current. The output voltage and current waveform qualities are noticed to degrade with increase of W in correspondence with the decrease of the MLVR-VSC reactive power generation.

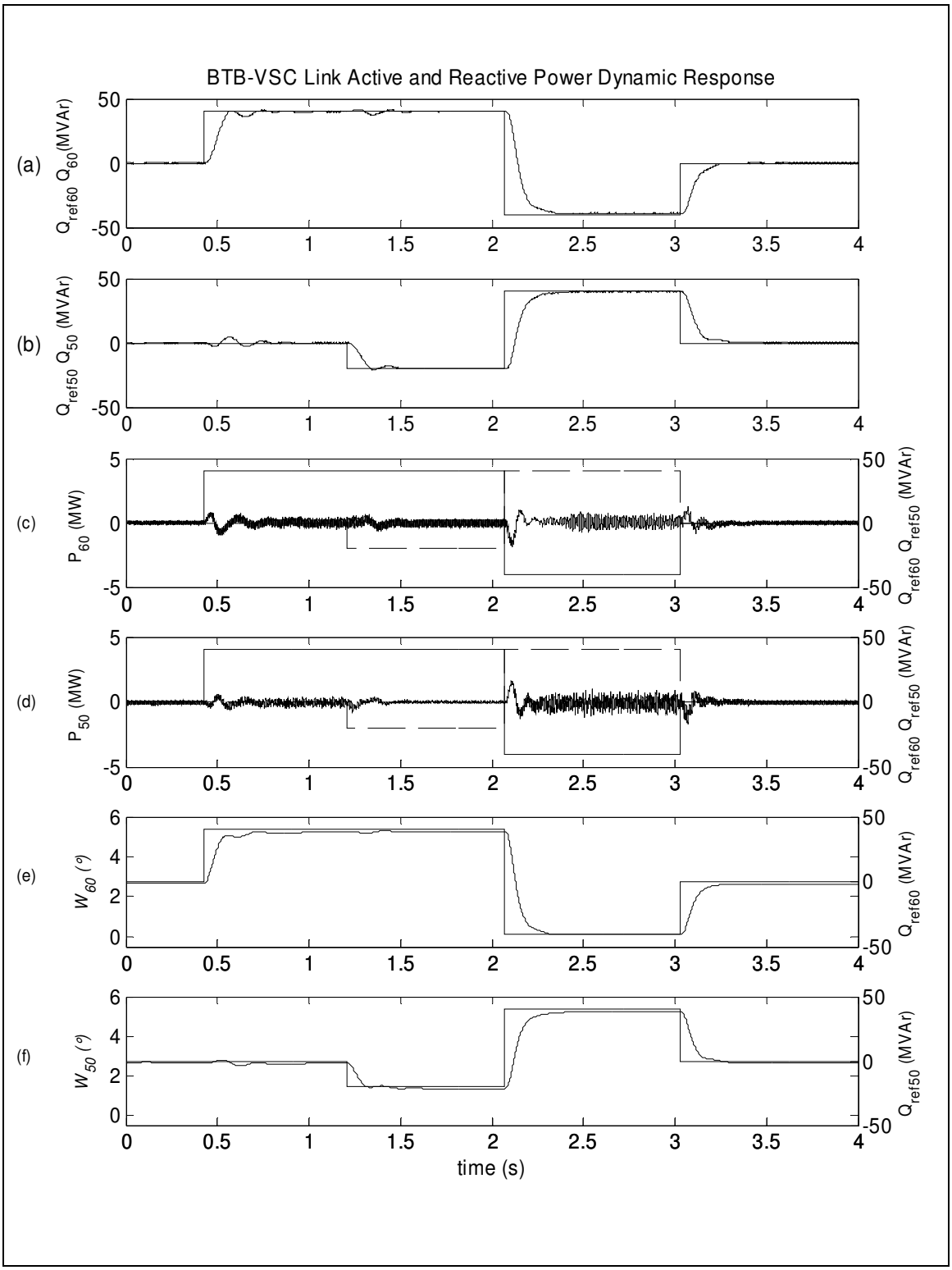


Figure 5.17 Active and reactive power responses to reactive power order.

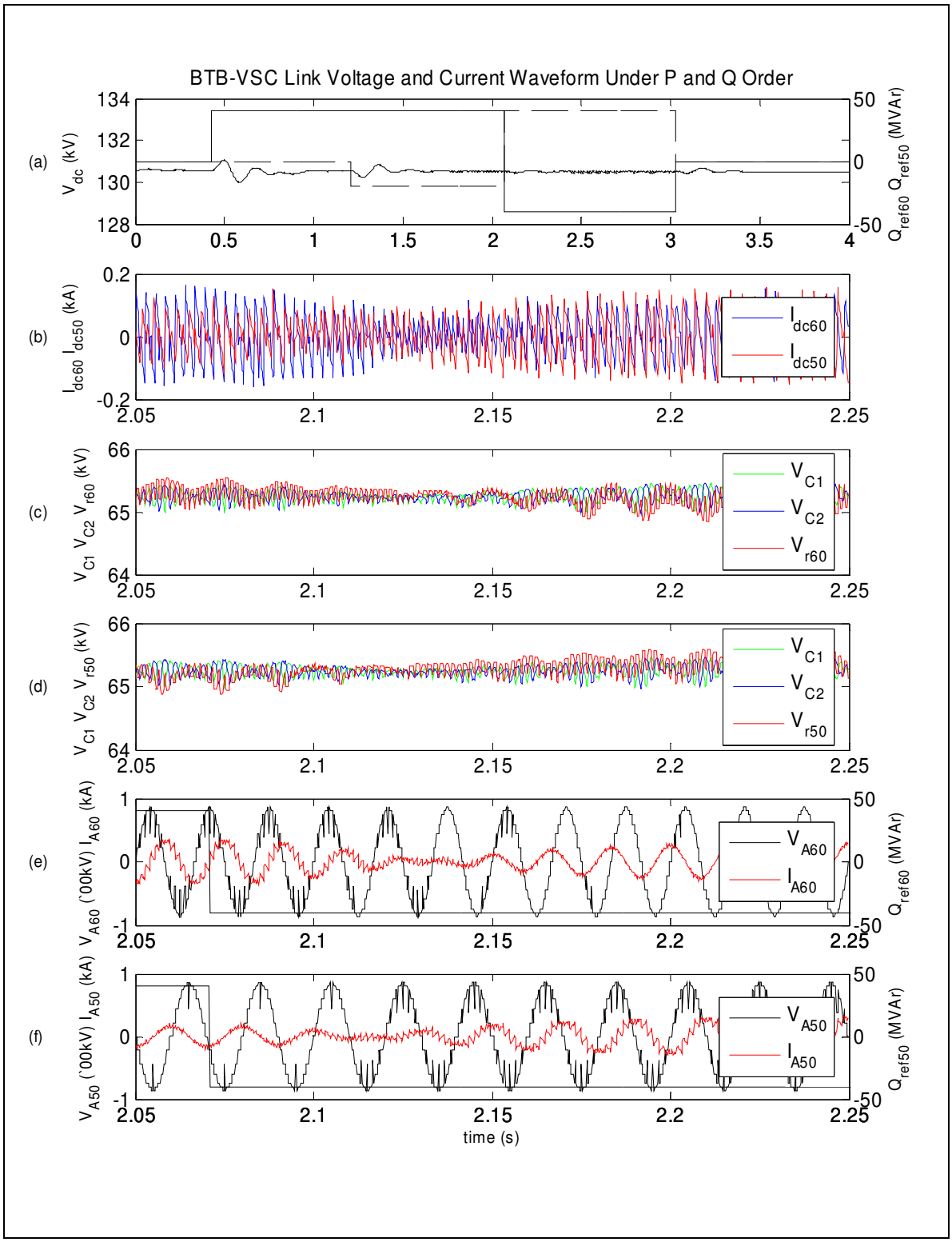


Figure 5.18 Voltage and current responses to reactive power order.

5.4.3.3 DC Bus Voltage Response

Figure 5.19 and 5.20 show the BTB-VSC link dynamic response under normal conditions to dc bus voltage reference step changes. The BTB-VSC is operated to transfer 80MW active power from the 60Hz system to the 50Hz system and consume -30MVAr and 30MVAr reactive powers from the 60Hz and 50Hz system respectively. Initially, the dc bus voltage is at steady-state value of 130.5kV. After t=0.5s, the dc bus voltage reference is increased to 138kV. At t=1.25s, the reference value is set to 126kV, and after t=3s, it is set back to 130.5kV. The plots in figure 5.19 show the dynamic behaviour of the dc bus voltage and the BTB-VSC link for the period of $0<t<4$s. The plots in figure 5.20 show the dc side voltage and current waveforms which are:

(a) V_{dc}, the dc bus voltage (across two main dc capacitors, C_1 and C_2);
(b) I_{dc60} and I_{dc50}, the dc output currents of the 60Hz and 50Hz system side converters;
(c) I_{C1} and I_{C2}, the current into the dc main capacitors of C_1 and C_2 respectively;
(d) I_{Cr60}, the current into the 60Hz side MLVR-VSC H-bridge capacitor;
(e) I_{Cr50}, the current into the 50Hz side MLVR-VSC H-bridge capacitor;
(f) V_{C1}, V_{C2} and V_{r60}, the voltages of the dc main capacitors across Y/ Δ and Y/Y main bridge respectively and 60Hz side MLVR-VSC H-bridge capacitor;
(g) V_{C1}, V_{C2} and V_{r50}, the voltages of the dc main capacitors across Y/ Δ and Y/Y main bridge respectively and 50Hz side MLVR-VSC H-bridge capacitor.

In figure 5.19, the dc voltage takes about 0.4s to reach 98% of the set point value and transients are caused on the active and reactive powers following a dc bus voltage reference step change. It is noticeable that the dynamics on the 60Hz side active power are higher than those in 50Hz side active power. This is due to the fact that the dc bus voltage controller is cascaded to the 60Hz side active power control loop. The dynamics on the 50Hz side active power are caused by interactions between the 60Hz and 50Hz systems.

Because the reactive power generations are highly dependent on the MLVR-VSC output voltage fundamental component, which is directly dependent on the dc bus voltage and the modulation notches width, the dynamics on the Qs are much higher than those seen on Ps. As already mentioned, the voltage fundamental amplitude control is limited in this BTB-VSC system. When V_{dc} is too high, for periods of $0.5\text{s}<t<1.25\text{s}$ and $2.15\text{s}<t<3\text{s}$, the

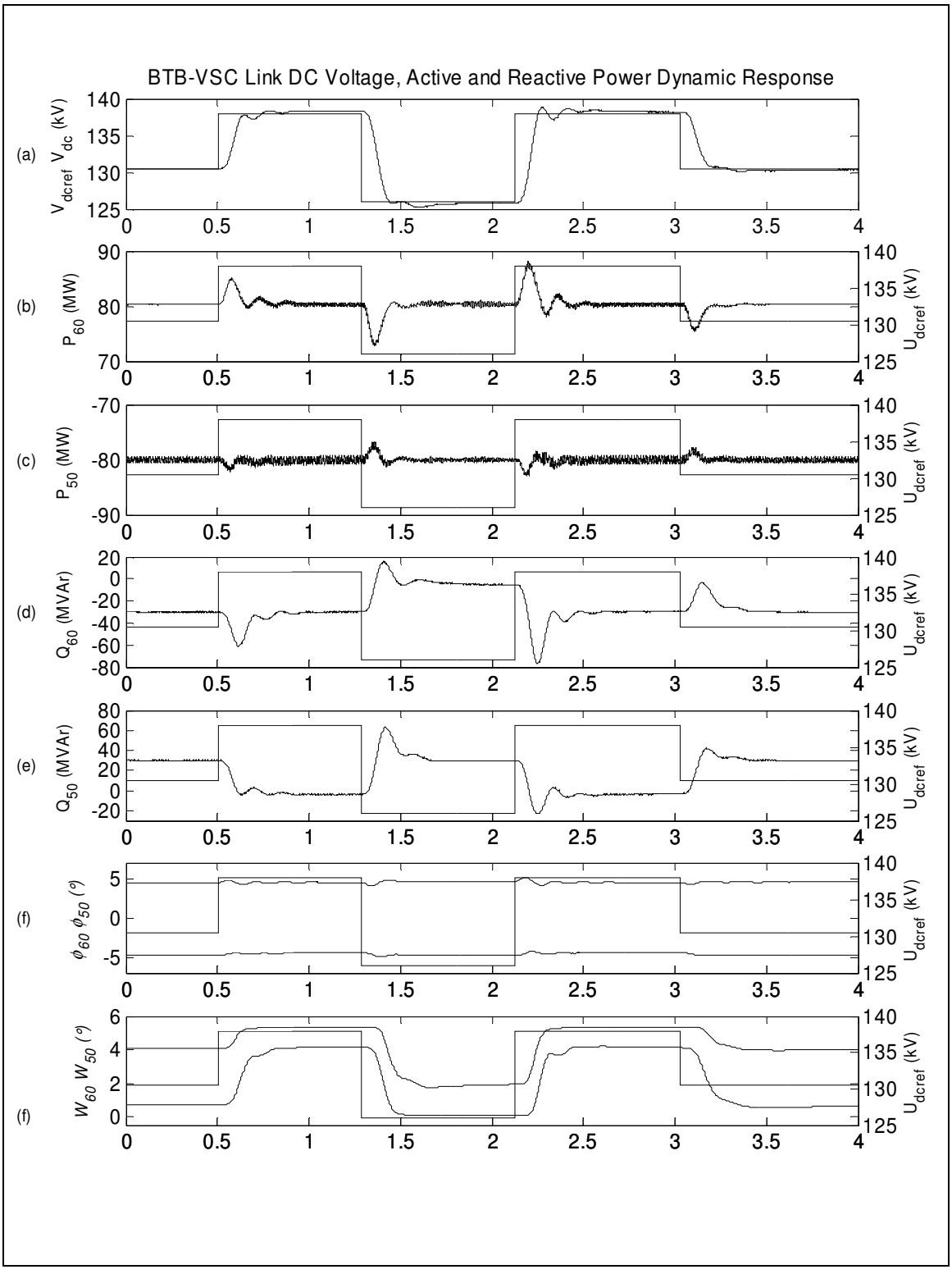


Figure 5.19 Dc bus voltage, active and reactive power responses to V_{dc} order.

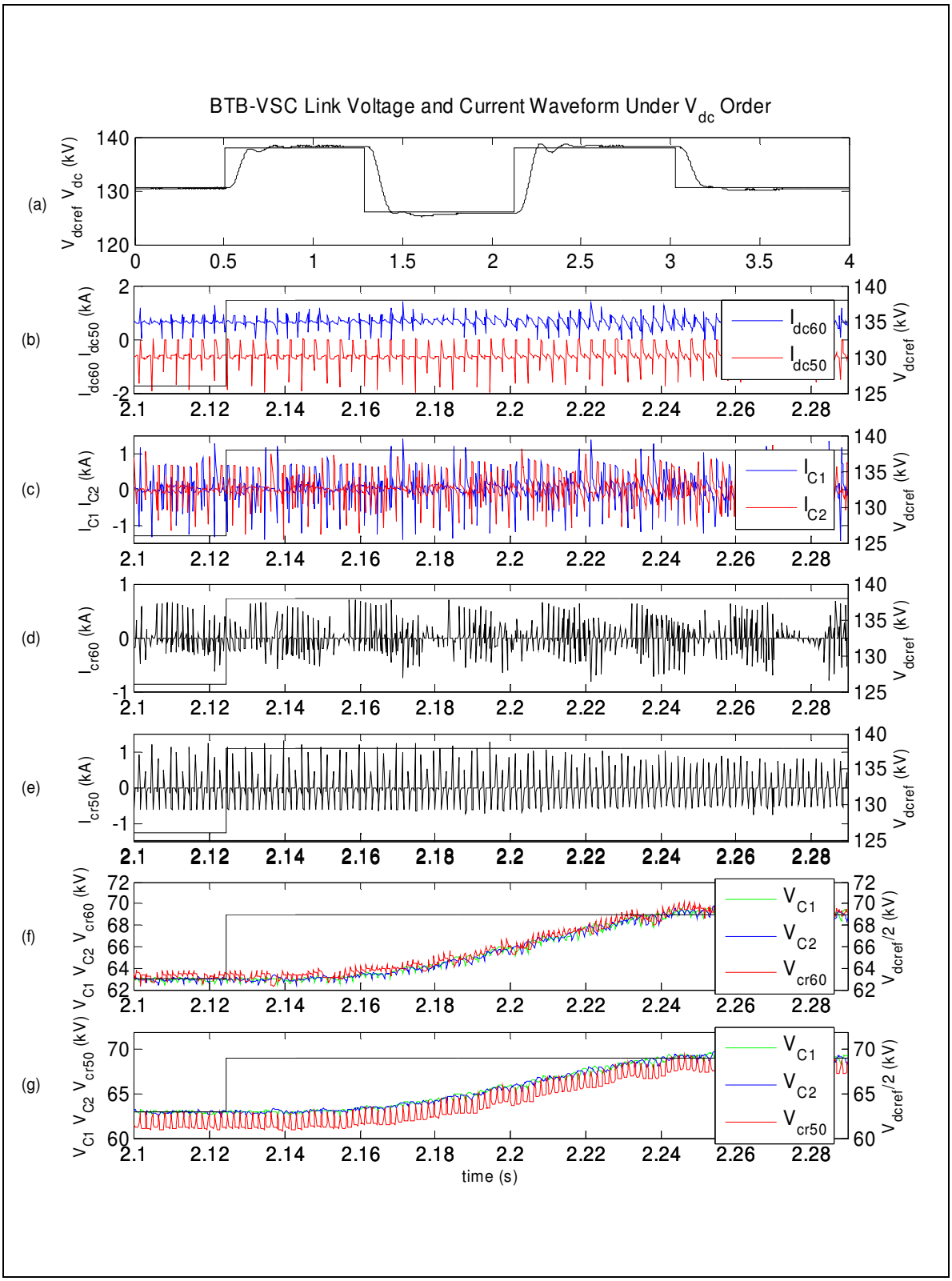


Figure 5.20 Voltage and current responses to V_{dc} order.

50Hz side MLVR-VSC which was initially consuming 30MVAr reactive power from the power system is forced to supply reactive power of 8MVAr into the power system. Its modulation notches width, W_{50}, at these periods saturates to a maximum value of 5°. For periods of $1.25<t<2.15$s, the V_{dc} is too low and thus the 60Hz side MLVR-VSC is forced to reduce the reactive power generation from initial value of 30MVAr to 5MVAr. Its modulation notches width, W_{60}, at this period saturates to a minimum value of 0°.

Waveforms of I_{dc60}, I_{dc50}, I_{C1}, I_{C2}, I_{Cr60}, I_{Cr50}, V_{C1}, V_{C2}, V_{r50} and V_{r60} are shown in greater detail in figure 5.20 for the interval of $2.1<t<2.3$s in order to show the dynamic process more clearly. Plots 5.20(f) and 5.20(g) show that all the capacitor voltages track well to each other but contain some ripples.

5.4.4 Cross Influence of Active and Reactive Powers

Figure 5.21 and 5.22 show the BTB-VSC system dynamics under $\pm$80MW active power transfer order change, while the reactive power generations on both side are held relatively constant. The 60Hz side MLVR-VSC generates 30MVAr and consumes 30MVAr reactive power for periods of $0.1<t<3.6$s and $3.6<t<8$s respectively. The 50Hz side MLVR-VSC consumes 30MVAr and generates 30MVAr reactive power for periods of $0.1<t<3.6$s and $3.6<t<8$s respectively. Figure 5.23 and 5.24 show the BTB-VSC system dynamics under $\pm$30MVAr reactive power generation order change for both side MLVR-VSC while the active power transfer is held relatively constant. The active power transfer is 80MW from 60Hz to 50Hz system and 80MW from 50Hz to 60Hz system for periods of $0<t<3.5$s and $3.5<t<7.5$s respectively.

All these waveforms show that the reactive power generation order change causes negligible transients on the active power transfer. Active power transfer order change, on the other hand, cause larger but not significant transients on both side's reactive powers. The largest reactive power transient caused by the cross influence of P and Q is recorded for 50Hz side MLVR-VSC at period around 3.5s in figure 5.23. This is when the active power transfer is changed from 80MW, from 60Hz to 50Hz system, to 80MW, from 50Hz to 60Hz system. Throughout all the power orders changes, including a 2 p.u. power change, both MLVR-VSCs did not experience over current.

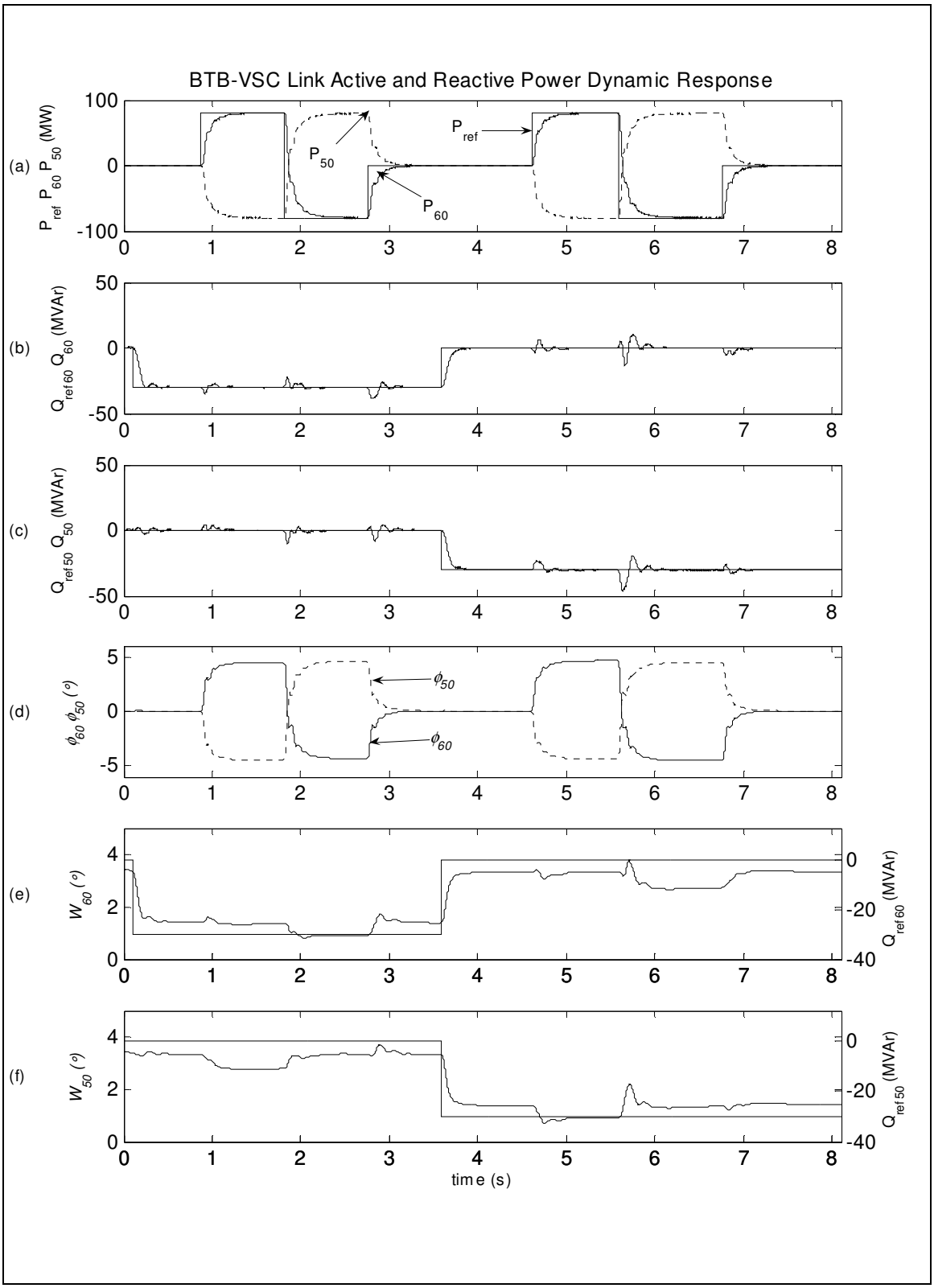


Figure 5.21 Active and reactive power responses to active and reactive power orders.

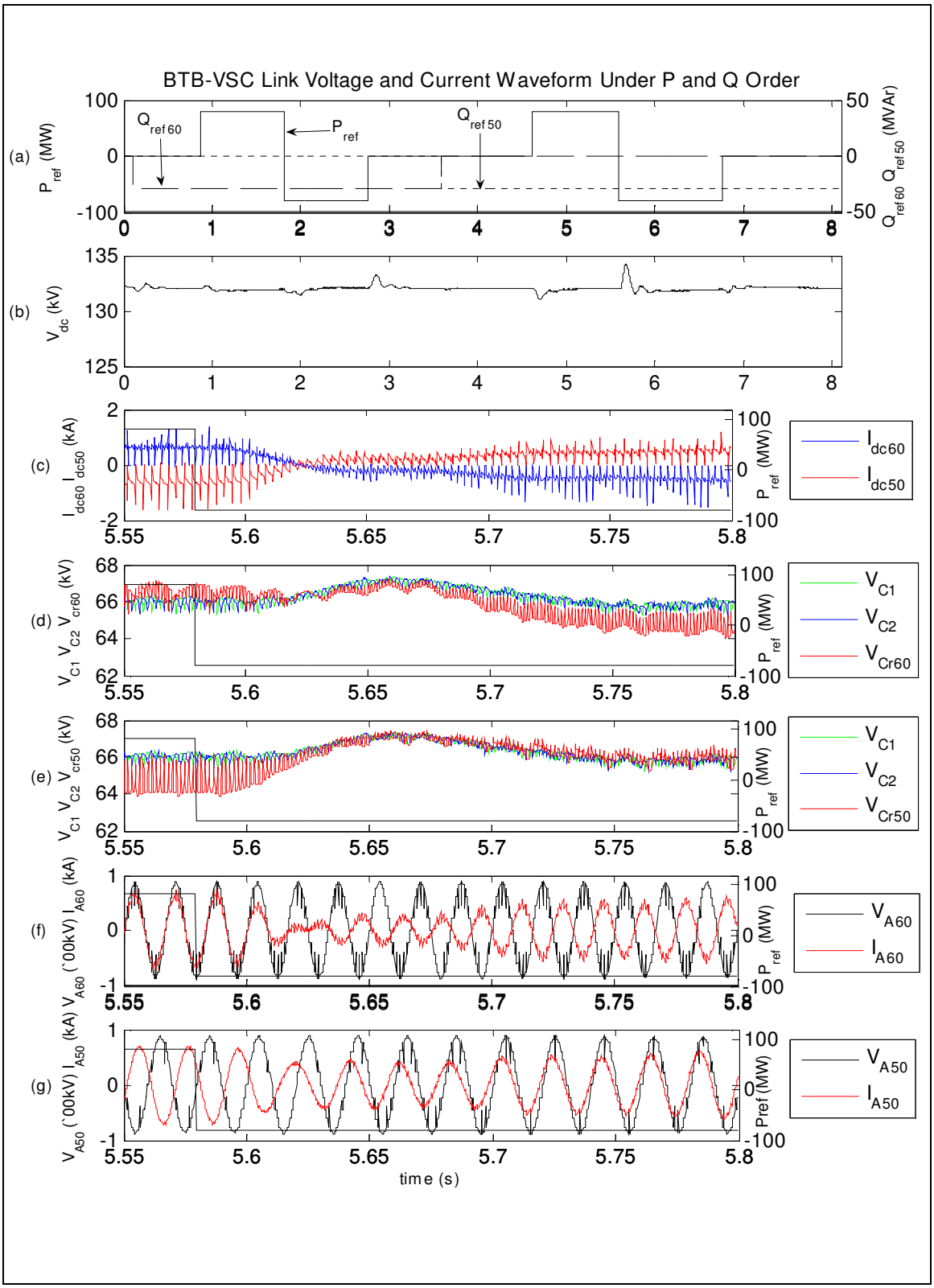


Figure 5.22 Voltage and current responses to active and reactive power orders.

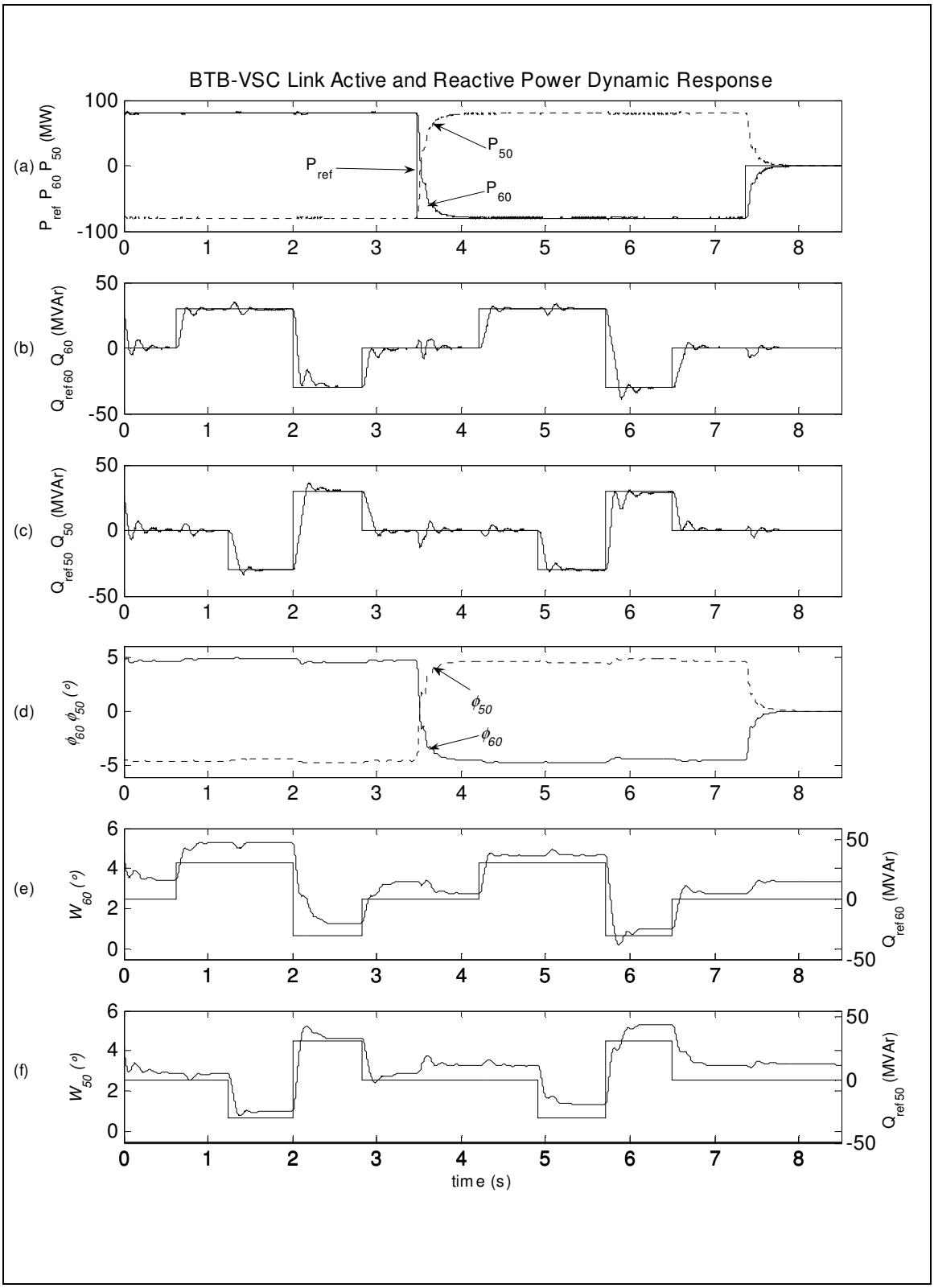


Figure 5.23 Active and reactive power responses to active and reactive power orders.

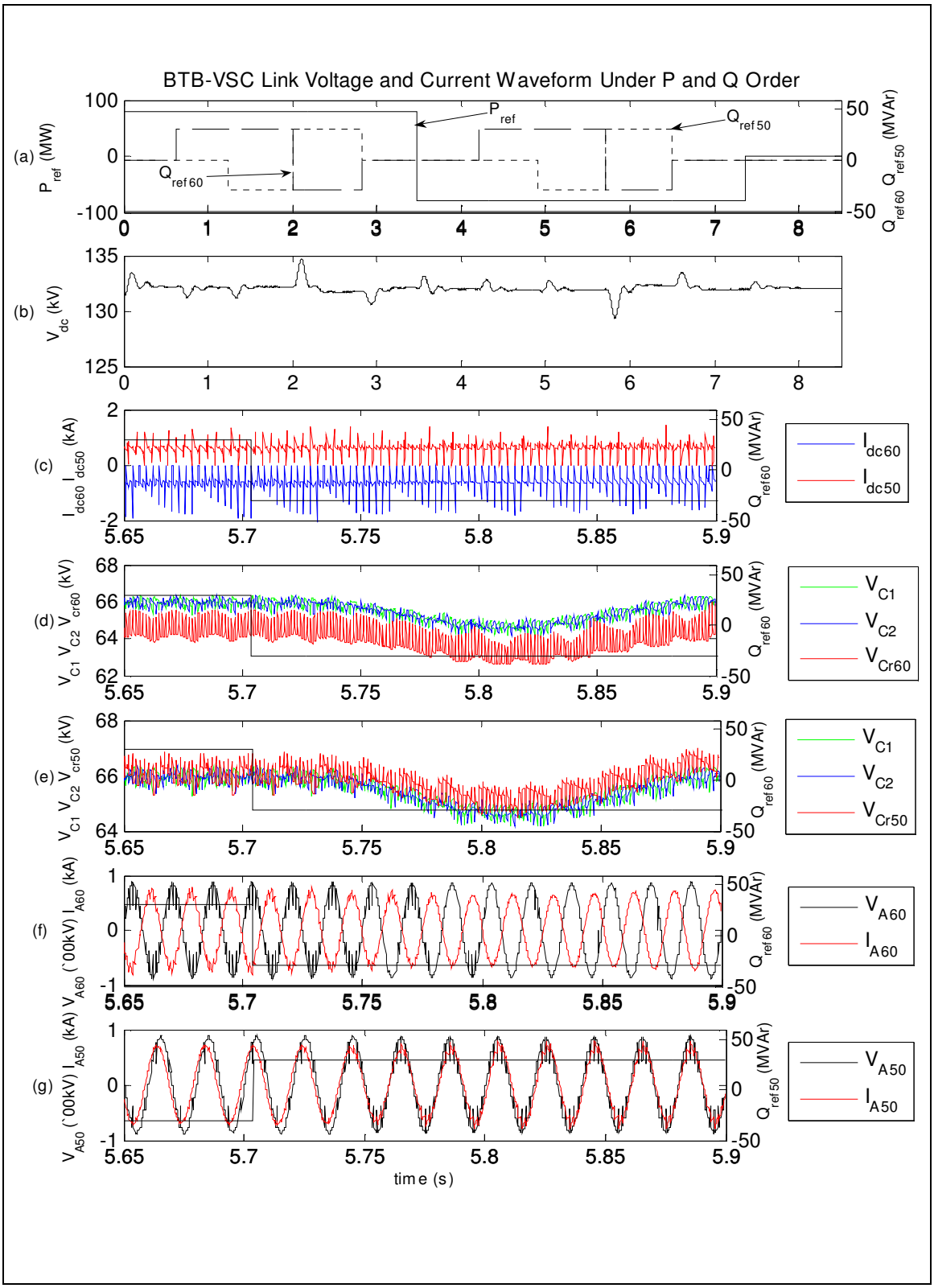


Figure 5.24 Voltage and current responses to active and reactive power orders.

5.4.5 Cross Modulation of a Fully Asynchronous System

The capacitor voltages plots in figure 5.15-5.24 are not as “clean” as those shown for stand-alone MLVR-VSC simulation. In the case of the BTB-VSC 60-50Hz link, the simulated capacitor voltages show small amplitude oscillations in the 60-80Hz frequency range. It is likely that these oscillatory ripples are caused by the inter-modulation between the 60Hz and 50Hz systems. Because the effects on the ac outputs on both side power systems are not significant, this matter is not investigated further in this report.

5.5 Conclusion

The functionality of the MLVR-VSC has been verified in this chapter through simulations based on two models, one of stand-alone basis and the other of a dc interlink. The stand-alone model provide results which correspond with the analysis discussed in previous chapters from waveform shapes to current flows within the converter. A fully asynchronous back-to-back HVdc link using the MLVR-VSC as its building block has been investigated for controllability and flexibility. These objectives are met for terminals of the link can be controlled to transfer bi-directional active power and generate reactive power independently.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The reinjection concept's fundamental objective is to inject triplen harmonics on the dc side of an ac-dc converter in order to cancel some of the ac harmonics. Recently, based on the reinjection technique, a new concept of ac-dc conversion suitable for high power applications was developed. It offers the advantages of low harmonic content output, efficient bridge commutation and no dynamic voltage sharing problem between switches connected in series. However, strict adoption of this concept to a voltage source converter (VSC) will yield ac voltage waveforms which are rigidly related to the dc bus voltage. While this is not a disadvantage when the converter is operated in a stand-alone manner, applications such as HVdc transmission systems where the dc bus voltage is globally shared by all its terminal converters is a limiting factor.

This thesis has proposed a way to control the multi-level voltage reinjection voltage source converter (MLVR-VSC) output voltage without varying the dc bus voltage. It is achieved by notching the MLVR-VSC ac output voltage waveforms so that the Fourier component magnitudes can be varied. The main interest is in its ability to modulate the fundamental component amplitude so that the reactive power generated (or absorbed) by the MLVR-VSC can be varied even when the dc bus voltage is constant.

Unlike the conventional modulation method via converter bridge chopping actions, as in the case of the pulse width modulation concept (PWM), the modulation notches are introduced directly on the dc side voltage waveforms which will then be coupled onto the ac side. Thus the MLVR-VSC advantages of zero voltage switching (ZVS), low *dV/dt* stress across the bridge, no dynamic voltage sharing problem between series connected switches in a valves can be preserved for high power, high voltage applications. Consequently, from the restrictions imposed by the harmonics cancellation concept and the complimentary nature of the converter bridges, notched top trapezoidal waveforms are applied to the converter dc side. This waveform shape

is modified from the linear triangular reinjection waveform shape deduced by Liu. The MLVR-VSC output voltage waveform resembles a sinewave with 12 regular notches. By adjusting the width of these notches, limited MLVR-VSC output voltage can be achieved. The depth of the notches, however, is usually restricted by the topological structure of the converter.

Harmonic analysis of the voltage waveforms of the modulated MLVR-VSC has been performed by assuming three phase balanced condition, infinite dc side capacitance, zero turn on (off) time and zero voltage drops for the valves. Two aspects of converter harmonic performance have been investigated, i.e. the converter output voltage and current. Harmonic voltage results for modulation levels from zero up to a maximum, where the reactive power generation flexibility is 1 p.u., show that there is significant increase of low order harmonics; some of which even consist of up to 23% of the fundamental component when the notches depth is deep. Harmonic current penetration into the power system is dependent on the filtering effects present between the power system source and the MLVR-VSC output voltage. The results presented are of an investigation for the lowest possible filtering effect, where the reactance between the MLVR-VSC voltage waveform and the power system source is solely due to the interface transformer leakage reactance.

The circuit which is used to synthesize the notched trapezoidal waveform was modified from the conventional cascaded H-bridge topology used to interface separated dc source to the grid. A complete MLVR-VSC consists of a general 12-pulse converter and the cascaded H-bridges being placed from the converter neutral point to the mid point across the dc bus. Each H-bridge dc capacitor contributes to one voltage step level on the waveforms and the cascade chain is common to, but imposes opposite voltages across, the two 6-pulse converters used to build the 12-pulse converter. An advantage of this topology is that the total number of switches required is significantly less than other currently available topologies which permit unity power factor operation and synthesis flexibility. A prospective advantage is that the H-bridge switch states redundancy can be exploited for capacitor voltage balancing purposes, although work in this direction has not been carried out.

The complementary nature of the 6-pulse converters causes bulging of one converter's waveforms when notches are introduced on waveforms of the other. If these bulges are allowed to be reflected onto the ac side, they will annihilate the modulation notches. Another issue pertinent to this topology is the tracking of the H-bridge capacitor voltages to the dc bus voltage. These two issues have been resolved

by modifying the 12-pulse converter switching functions to avoid complementary bulges from being reflected onto the ac side, and also to provide a bypass to enforce voltage sharing between the reinjection branch and the main dc capacitors. A side effect from breaking the dc side current loop during bulge elimination is that each 6-pulse converter current is alternately diverted into the reinjection branch. This leads to the current rating increase of the circuit elements on the reinjection branch. Voltage sharing bypass will cause current spikes whenever there is a difference between reinjection voltage and main dc capacitor voltages. An inductor is deliberately added on the reinjection branch to limit these current spikes.

The 12-pulse converter valves commutate under zero voltage conditions and so their switching losses are minimal and snubber requirements are simple. However, this is not the case for the H-bridges valves. The H-bridges are hard-switched in order to connect their capacitors positively, negatively or neutrally. Fortunately, the H-bridges are rated at only a fraction of the dc bus voltage and hence their switching losses are low. Overall, the MLVR-VSC is a more efficient converter than the PWM based VSC.

PSCAD/EMTDC simulation results for a stand-alone MLVR-VSC model shows satisfactory similarity to the analytical waveforms. Dc side currents and capacitor voltages when the MLVR-VSC is converting active power have higher ripples and peaks than when it is only generating reactive power. This phenomenon is associated with the current diversion into the reinjection branch when active power operation involves some dc average component.

The extension of the stand-alone MLVR-VSC to a back-to-back HVdc transmission system is simple. Each terminal consists of a 12-pulse converter interfaced to the grid with two sets of transformers (Y/Y and Y/Δ configured) and an H-bridge. Both terminals share two common dc capacitors which are connected across the dc bus. Four control loops have been deduced using control block diagrams which involve only the fundamental components. Safe operating and steady-state operating regions of the HVdc system were determined with studies performed for phasor relationships between these components.

Finally, the dynamic control performance, active and reactive power flow control flexibility of a fully asynchronous back-to-back HVdc system was verified by simulation. The response of the link to step changes in reactive power generations, active power transfer and dc bus voltage command orders is satisfactory but with

some imperfections. From the results presented, there is a cross-influence between converter active power and reactive power flows. The P step change influence on Q loops is clearly observable while the Q step change influence on P loops is negligibly small. Also, non-significant voltage oscillation between 70Hz and 80Hz frequency is observable. These oscillations are likely to be caused by cross modulations between the 50Hz and 60Hz systems.

6.2 Future Work

The MLVR-VSC has been extended in this thesis for a fully asynchronous back-to-back HVdc application with independent reactive power generation. Further investigations into the converter characteristics are needed especially around the dynamics of the converter. This study is essential for optimising the component values and develops a suitable control structure for the converter. In this thesis, the functionality of the link has been proven by EMT simulations accuracy of which is assessed by examining waveform similarities and consistencies with the analytical current flow paths. In order to predetermine the component values to match specific application, precise correlation between the inductance, capacitance and converter operation condition needs to be known. As for the control system performance, the response of the HVdc system to transient events not only depends on the converter characteristics but also those of the ac networks connected to the HVdc terminals. It would require a fair amount of understanding of the realistic networks in order to draw the boundary line for reactive power requirements and to estimate grid influences on the converter operation and vice versa. The following sections discuss some possible future developments in continuing the work carried out in this thesis.

6.2.1 MLVR-VSC Dynamics Studies and Component Optimisation

The current spike limiting inductor, H-bridge capacitor and main dc bus capacitors in the MLVR-VSC are implemented only with one set of component values chosen from many trials and errors. However, they are by no means the only or optimised set of component values. Because the spikes and ripples are sensitive to both control loop performance and the converter operation condition, it is difficult to determine an accurate correlation between the current spikes, the voltage ripples and the component values. Further effort is needed to obtain the boundary conditions of state space equations governing the converter dynamics so that the component values can be

optimised for least current spikes and capacitor voltage ripples. Only then can the ratings of the circuit elements in the MLVR-VSC be calculated inclusively.

6.2.2 Multiple Cascaded H-bridges and Balancing Their Capacitor Voltages

The constructed simulation model in this thesis has only one H-bridge in order to avoid complexity in H-bridge valves firing patterns. This shortcoming has to be overcome if the converter output waveform quality is to be improved by having more cascaded H-bridges on the reinjection branch to synthesize more step levels. The organisation of multiple H-bridge switch state combinations becomes very complex as the number of possible switch state combination increases phenomenally with the number of H-bridges. The organisation not only has to maintain equal capacitor voltages during steady-state, it should also have self-deterministic capability to allow the capacitor voltages to recover following transient events. To complicate things further, notchings on MLVR-VSC waveforms have caused part of the main bridge currents to be diverted into the reinjection branch momentarily. This makes the charging and discharging effects of H-bridge capacitors very sensitive to the converter operation condition.

6.2.3 Modelling and Control Structure of the Converter

The control blocks and phasor diagrams presented in this thesis only consider the fundamental components for steady-state operation with three phase balance and an ideal power system. This has the danger of disregarding the effects that an actual grid has on the converter operation, may it be load fluctuations, network resonance oscillations or busbar faults. Voltage oscillation between the 70Hz and 80Hz can be clearly seen on the results presented. Though it is not significant for the case shown, its effects in other cases are unknown. Additionally, the cross influence of the P and Q loops have to be studied further and, hopefully, a method derived to mitigate this effect or even eliminate it totally. However, before control strategies to overcome these problems can be developed, comprehensive modelling of the converter has to be performed in awareness that the EMT simulation packages are far from perfect. They very often have the tendency to hide important characteristics from the user and sometimes even give erroneous solutions.

6.2.4 Generalised Overview of the MLVR-VSC

Obviously, fundamental voltage modulation to control reactive power flow is only needed for MLVR-VSC when it is applied to nonflexible dc bus voltage applications such as an HVdc transmission system. In the stand-alone version, MLVR-VSC output voltage can be directly controlled by varying the dc bus voltage. The reactive power compensation required from an HVdc converter is dependent on the characteristics of the power system to which it is connected and is limited by the current ratings of the converter. Under normal operation, the current into an HVdc terminal should consists mostly of active power components. Moreover, the HVdc link terminal should only generate enough reactive power to support the terminal busbar voltage and perform power factor correction. Remote inductive loads should be compensated locally so that reactive current flows are limited, reducing transmission losses. Hence, it is very important to perform a study from the power system point of view in order to appreciate just how much the converter waveform quality needs to be compromised, in conjunction with the modulation level required, to achieve independent reactive power generation. This will lead to a complete overview of possible application areas of the modulated MLVR-VSC and a precise performance comparison with other high voltage converters.

APPENDIX A

The Harmonic Concept and Its Symmetrical Approximation [24]

A.1 The Harmonic Cancellation Concept

Let $V_{YY}(\omega t)$ be the voltage across the dc side terminal of the Y/Y bridge of a 12-pulse converter and $V_{Y\Delta}(\omega t)$ be the voltage across the dc side terminal of the Y/Δ bridge of a 12-pulse converter. Following the standard 180° firing pattern for a 12-pulse VSC, the secondary windings of the two interface transformers on the bridges side are give by

$$V_{YA}(\omega t)=\begin{cases} V_{YY}(\omega t)/3 & for \quad 0<\omega t<\pi/3; \\ 2V_{YY}(\omega t)/3 & for \quad \pi/3<\omega t<2\pi/3; \\ V_{YY}(\omega t)/3 & for \quad 2\pi/3<\omega t<\pi; \\ -V_{YY}(\omega t)/3 & for \quad \pi<\omega t<4\pi/3; \\ -2V_{YY}(\omega t)/3 & for \quad 4\pi/3<\omega t<5\pi/3; \\ -V_{YY}(\omega t)/3 & for \quad 5\pi/3<\omega t<2\pi. \end{cases} \tag{A.1.1}$$

$$V_{\Delta A}(\omega t)=\begin{cases} 0 & for \quad 0<\omega t<\pi/6; \\ V_{Y\Delta}(\omega t) & for \quad \pi/6<\omega t<5\pi/6; \\ 0 & for \quad 5\pi/6<\omega t<7\pi/6; \\ V_{Y\Delta}(\omega t) & for \quad 7\pi/6<\omega t<11\pi/6; \\ 0 & for \quad 11\pi/6<\omega t<2\pi. \end{cases} \tag{A.1.2}$$

If $V_{YY}(\omega t)=U_{dc}+A_{Ym}\cos(m\omega t)+B_{Ym}\sin(m\omega t)$ and
$V_{Y\Delta}(\omega t)=U_{dc}+A_{\Delta m}\cos(m\omega t)+\mathrm{B}_{\mathrm{Y}\Delta}\sin(m\omega t)$,

the Fourier components of Y/Y connected transfromer secondary winding voltage $V_{YA}(\omega t)$ are given by

$$\begin{aligned} V_{YAn} &= \frac{2}{\pi}\left[\int_0^{\pi}\frac{V_{YY}(\omega t)}{3}\sin(n\omega t)d\omega t+\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}}\frac{V_{YY}(\omega t)}{3}\sin(n\omega t)d\omega t\right] \\ &= V_{dcYAn}+V_{\cos YAn}+V_{\sin YAn} \end{aligned} \tag{A.1.3}$$

$$V_{dcYAn} = \frac{4\left[1-(-1)^n\right]}{3n\pi} U_{dc} \cos^2\left(\frac{n\pi}{6}\right) \tag{A.1.4}$$

$$V_{\cos YAn} = \begin{cases} \dfrac{\left[1-(-1)^{n+m}\right]A_{Ym}}{3\pi}\left[\dfrac{2n}{n^2-m^2} + \dfrac{1}{n+m}\cos\left(\dfrac{(n+m)\pi}{3}\right) + \dfrac{1}{n-m}\cos\left(\dfrac{(n-m)\pi}{3}\right)\right] & (m \neq n) \\ 0 & (m = n) \end{cases}$$

(A.1.5)

$$V_{\sin YAn} = \begin{cases} \dfrac{\left[1-(-1)^{n+m}\right]B_{Ym}}{3\pi}\left[\dfrac{1}{n+m}\sin\left(\dfrac{(n+m)\pi}{3}\right) - \dfrac{1}{n-m}\sin\left(\dfrac{(n-m)\pi}{3}\right)\right] & (m \neq n) \\ \dfrac{1}{3\pi} B_{Ym}\left[\dfrac{4\pi}{3} - \dfrac{(-1)^m}{2m}\sin\left(\dfrac{m\pi}{3}\right)\right] & (m = n) \end{cases}$$

(A.1.6)

Similary, the Fourier components of the Y/Δ connected transformer secondary winding voltage $V_{\Delta A}(\omega t)$ are given by

$$\begin{aligned} V_{\Delta An} &= \frac{2}{\pi}\int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} V_{Y\Delta}(\omega t)\sin(n\omega t)d\omega t \\ &= V_{dc\Delta An} + V_{\cos\Delta An} + V_{\sin\Delta An} \end{aligned} \tag{A.1.7}$$

$$V_{dc\Delta An} = \frac{2\left[1-(-1)^n\right]}{n\pi} U_{dc} \cos\left(\frac{n\pi}{6}\right) \tag{A.1.8}$$

$$V_{\cos\Delta An} = \begin{cases} \dfrac{\left[1-(-1)^{n+m}\right]A_{\Delta m}}{\pi}\left[\dfrac{1}{n+m}\cos\left(\dfrac{(n+m)\pi}{6}\right) + \dfrac{1}{n-m}\cos\left(\dfrac{(n-m)\pi}{6}\right)\right] & (m \neq n) \\ 0 & (m = n) \end{cases}$$

(A.1.9)

$$V_{\sin\Delta An} = \begin{cases} \dfrac{\left[1-(-1)^{n+m}\right]B_{\Delta m}}{\pi}\left[\dfrac{1}{n+m}\sin\left(\dfrac{(n+m)\pi}{6}\right) - \dfrac{1}{n-m}\sin\left(\dfrac{(n-m)\pi}{6}\right)\right] & (m \neq n) \\ \dfrac{1}{\pi} B_{\Delta m}\left[\dfrac{2\pi}{3} + \dfrac{1}{m}\sin\left(\dfrac{m\pi}{3}\right)\right] & (m = n) \end{cases}$$

(A.1.10)

The Fourier expression of V_{dcYAn} indicates that the harmonics produced by the dc component are of orders $n=6l\pm1$ (l=1,2,3…). The harmonic spectrum of V_{cosYAn} depends on the frequency of the corresponding bridge voltage component $A_{Ym}(m\omega t)$; if $m=6k$ (k=1,2,3…),

$$V_{\cos YAn} = \frac{\left[1-(-1)^n\right]}{3\pi} A_{Ym}\left[\frac{2n}{n^2-36k^2} + \frac{1}{n+6k}\cos\left(\frac{n\pi}{3}\right) + \frac{1}{n-6k}\cos\left(\frac{n\pi}{6}\right)\right]$$

$$= \frac{\left[1-(-1)^n\right]}{3\pi} A_{Ym}\left[\frac{2n}{n^2-36k^2} + \frac{2n}{n^2+36k^2}\cos\left(\frac{n\pi}{3}\right)\right]$$

$$= \frac{4n\left[1-(-1)^n\right]}{3\pi\left(n^2-36k\right)} A_{Ym}\cos^2\left(\frac{n\pi}{6}\right) \qquad \text{(A.1.11)}$$

This indicates that its harmonic components are of the same orders as those of V_{dcYAn}. By choosing the appropriate amplitude of $A_{Ym}\cos(m\omega t)$ and freqency factor $m=6k$ (k=1,2,3…), the harmonic components of the secondary windings voltage part $V_{dcYA}(\omega t)$ can be modified, i.e. harmonics of some orders can be decreased while those of other orders increased.

V_{sinYAn} contains evern order harmonics, which is undesirable, and therefore the voltage across the bridge connected to the Y/Y transformer will not include the component $B_{Ym}\sin(m\omega t)$.

The spectrum of $V_{cos\Delta An}$ depends on the frequency of the corresponidng bridge voltage component $A_{\Delta m}(m\omega t)$; if $m=6k$ (k=1,2,3…),

$$V_{\cos \Delta An} = \frac{\left[1-(-1)^n\right]}{\pi} A_{\Delta m}\left[\frac{(-1)^k}{n+6k}\cos\left(\frac{n\pi}{6}\right) + \frac{(-1)^k}{n-6k}\cos\left(\frac{n\pi}{6}\right)\right]$$

$$= \frac{(-1)^k\left[1-(-1)^n\right]}{\pi} A_{\Delta m}\left[\frac{1}{n+6k} + \frac{1}{n-6k}\right]\cos\left(\frac{n\pi}{6}\right)$$

$$= \frac{2n(-1)^k\left[1-(-1)^n\right]}{\pi\left(n^2-36k\right)} A_{\Delta m}\cos\left(\frac{n\pi}{6}\right) \qquad \text{(A.1.12)}$$

This indicates that its harmonic components are of the same orders as those of $V_{dc\Delta An}$. By choosing appropriate amplitude of $A_{\Delta m}\cos(m\omega t)$ and frequency factor m=6k (k=1,2,3…), the harmonic components of the secondary winding voltage part $V_{dc\Delta A}(\omega t)$ can be modified, i.e. harmonics of some orders can be decreased while those of other orders increased.

In the conventional 12-pulse configuration the harmonics of order n=6(2l-1)$\pm$1 (l=1,2,3…) of the Y/Y and Y/Δ interface transformer winding voltages $V_{YA}(\omega t)$ and $V_{\Delta A}(\omega t)$ are out of phase by 180°; while the harmonics of order n=12$l\pm$1 (l=1,2,3…) are in phase. If the voltage across the bridge connected to the Y/Y transformer is

$$V_{YY}(\omega t) = \frac{U_{dc}}{2} + \sum_{k=1}^{\infty} A_{Yk}\cos(6k\omega t) \qquad \text{(A.1.13)}$$

and the voltage across the bridge connected to the Y/Δ transformer is

$$V_{Y\Delta}(\omega t) = \frac{U_{dc}}{2} + \sum_{k=1}^{\infty} A_{\Delta k}\cos(6k\omega t) \qquad \text{(A.1.14)}$$

and if the corresponding winding voltages $V_{YA}(\omega t)$ and $V_{\Delta A}(\omega t)$ only include harmonics of order n=6(2l-1)$\pm$1 (l=1,2,3…), then the combination of the winding voltages on the interface transformer primary side will produce harmonic distortion-free voltage waveforms. To achieve this goal the relation between the dc component and ac components of the bridge voltages is given by the equations

$$\sum_{k=1}^{\infty}\frac{A_{Yk}}{(12l\pm1)^2-36k^2} = \frac{U_{dc}}{2(12l\pm1)^2} \qquad (l=1,2,3,\ldots) \qquad \text{(A.1.15)}$$

$$\sum_{k=1}^{\infty}\frac{(-1)^k A_{\Delta k}}{(12l\pm1)^2-36k^2} = \frac{U_{dc}}{2(12l\pm1)^2} \qquad (l=1,2,3,\ldots) \qquad \text{(A.1.16)}$$

For the cancellation of the primary side harmonics of orders n=6(2l-1)$\pm$1 (l=1,2,3…), the relation $(-1)^k A_{\Delta k}=A_{Yk}$ (k=1,2,3…) must be satisfied. Therefore the condition for harmonic cancellation in the 12-pulse reinjection VSC is simplified to that of equation A.1.15.

A.2 Symmetrical Approximation

The harmonic cancellation condition of the 12-pulse converter given in equation A.1.15 constitute a set of linear algebraic equations for determining infinite variables (A_{Yk}/U_{dc} k=1,2,3…).

In practice very high order harmonics are negligible and thus the number of equations can be reduced. If the harmonics in the output waveform of orders higher than (12m+1) are ignored, the equation number is reduced to 2m. With these 2m equations, the 2m or less variables (A_{Yk}, k=1,2,…,$m\leq 2m$) can be determined.

The numerical solutions of A_{Yk} for a sufficiently large value of the number m can be approximately expressed explicitly by

$$\frac{A_{Yk}}{U_{dc}}=\frac{2\left[2(-1)^k-\sqrt{3}\right]}{\left(2-\sqrt{3}\right)\left(36k^2-1\right)}\approx\frac{14.9282(-1)^k-12.9282}{36k^2-1}\quad (k=1,2,3,\ldots)\ \text{(A.2.1)}$$

and

$$\frac{A_{\Delta k}}{U_{dc}}=(-1)^k\frac{A_{Yk}}{U_{dc}}\approx\frac{14.9282-12.9282(-1)^k}{36k^2-1}\qquad\text{(A.2.2)}$$

Based on the numerical results of A_{Yk}, the normalised reinjection voltage waveforms of

$$X_Y(x)=1+\sum_{k=1}^{\infty}A_{Yk}\cos(6kx)\qquad\text{(A.2.3)}$$

and

$$X_\Delta(x)=1+\sum_{k=1}^{\infty}(-1)^k A_{Yk}\cos(6kx)\qquad\text{(A.2.4)}$$

are applied to the Y-connection and Δ-connection bridge. The two waveforms posses the following important characteristics

1. Zero value appear at the points where the switches in the bridge are turned on and off;
2. The derivatives of the waveforms are limited, particularly around the zero values where the power switches change their states;
3. The two waveforms add to a dc level with very low amplitude ripple.

To overcome the difficulty of providing a ripple controllable dc power source the reinjection waveform has to be fully symmetrical. The use of fully symmetrical waveforms with minimum errors with respect to the ideal reinjection waveforms will simplify the requirement applied to the dc supply without causing significant harmonic distortion at the converter output.

Based on the conditions of minimizing the harmonic distortion and simplifying the practical implementation, the following two types of waveforms are derived:

1. A waveform that minimizes the integration of the error square and the error derivative square (ESEDS), is the optimal approximation of the ideal reinjection waveform under the symmetry restriction.
2. A linearly raising and linearly falling waveform, which provides constant derivative and linear voltage increment and decrement, is the simplest for practical implementation.

The EDEDS symmetrical waveform, $X_{Ys}(x)$, is obtained by solving the minimixation of

$$\min\left\{\int_0^{\frac{\pi}{6}}\left[\left[X_Y(x)-X_{Ys}(x)\right]^2+\left(\frac{d\left[X_Y(x)-X_{Ys}(x)\right]}{dx}\right)^2\right]dx + \int_0^{\frac{\pi}{6}}\left[\left[X_\Delta(x)-X_{\Delta s}(x)\right]^2+\left(\frac{d\left[X_\Delta(x)-X_{\Delta s}(x)\right]}{dx}\right)^2\right]dx\right\}$$

under the conditions of symmetry and are equality between the two groups of curves, i.e.

$$X_{Ys}(x)+X_{\Delta s}(x)=2 \qquad \text{for } 0<x<\pi/6$$

and $$\int_0^{\frac{\pi}{12}} X_{Ys}(x)dx = \int_0^{\frac{\pi}{12}} X_Y(x)dx, \quad \int_{\frac{\pi}{12}}^{\frac{6}{12}} X_{Ys}(x)dx = \int_{\frac{\pi}{12}}^{\frac{6}{12}} X_Y(x)dx$$

$$\int_0^{\frac{\pi}{12}} X_{\Delta s}(x)dx = \int_0^{\frac{\pi}{12}} X_\Delta(x)dx, \quad \int_{\frac{\pi}{12}}^{\frac{6}{12}} X_{\Delta s}(x)dx = \int_{\frac{\pi}{12}}^{\frac{6}{12}} X_\Delta(x)dx$$

Based on the numerical results of the symmetrical waveforms, X_{Ys} and $X_{\Delta s}$ the Fourier components of the ESEDS symmetrical waveform $X_{Ys}(x)$ is approximately given by an explicit formula of

$$A_{ESEDSk} = \frac{\left(7+4\sqrt{3}\right)\left[1-(-1)^k\right]}{36k^2-1} \approx \frac{13.9282\left[1-(-1)^k\right]}{k^2} \qquad \text{(A.2.5)}$$

and waveform $X_{\Delta s}(x)$ can be obtained by the application of 30° phase-shift.

The Fourier components of the linear symmtrical waveform is given by

$$A_{LINk} = \frac{4\left[1-(-1)^k\right]}{k^2\pi^2} \approx \frac{0.4053\left[1-(-1)^k\right]}{k^2} \qquad \text{(A.2.6)}$$

The ESEDS and Linear Symmetrical Reinjection waveforms not only possess the advantagous characteristics of the ideal reinjection waveforms but can also be supplied by a constant dc power source. The cost of the approximation is a slight harmonic distortion at the converter ac output terminals. The harmonic spectrum and the THD for the ESEDS symmetrical reinjection waveforms are given by

$$\frac{V_{Asym-n}}{V_{Asym-1}} = \frac{\frac{1}{12k\pm1} - \frac{\pi\left(2+\sqrt{3}\right)}{12(12k\pm2)}}{1+\frac{\pi(\pi-3)\left(2+\sqrt{3}\right)}{72}} \approx \frac{0.9774625}{12k\pm1} - \frac{0.95502838}{12k\pm2} \qquad n=12k\pm1, \quad k=1,2,3\ldots \qquad \text{(A.2.7)}$$

$$THD_{VAsym} = \sqrt{\frac{2\left(2+\sqrt{3}\right)\pi^2}{72+\pi(\pi-3)\left(2+\sqrt{3}\right)}-1} \approx 1.0167787\% \qquad \text{(A.2.8)}$$

The harmonic spectrum and the THD for the linear symmetrical reinjection waveforms are given by

$$\frac{V_{Alin-n}}{V_{Alin-1}} = \frac{1}{n^2} \qquad n=12k\pm1, \quad k=1,2,3\ldots \qquad \text{(A.2.9)}$$

$$THD_{VAslin} = \sqrt{\sum_{k=1}^{\infty} \frac{1}{(12k-1)^4} + \sum_{k=1}^{\infty} \frac{1}{(12k+1)^4}}$$

$$= \sqrt{\frac{\pi^4\left(40+23\sqrt{3}\right)}{8\times12\times81} - 1} \approx 1.05532\% \qquad \text{(A.2.10)}$$

APPENDIX B

Multi-level VSC Topologies

B.1 Diode-Clamped Topology

Among the published multi-level converters, the most widely accepted topology in terms of application is the Neutral-Point-Diode-Clamped converter (NPC) [48]. It is nothing more than a 3-level version of the more generic diode-clamped topology. Figure B.1 shows the single pole circuit of the diode-clamped multi-level voltage source converter (MLDC-VSC) from 2-level up to 5-level. An *m*-level MLDC-VSC requires

$$N_{capacitor} = (m-1) \qquad \text{(B.1.1)}$$

capacitors on the dc bus and produces a waveform with *m* steps. To explain the operation of a MLDC-VSC, a 5-level single pole circuit, figure B.1(c), is chosen as an example.

Each capacitor voltage is $V_{dc}/4$ since there are four series connected dc capacitors across the dc bus. The clamping diodes, D_{1a}-D_{3d}, clamp each switches, S_1-S_4 and S_1'-S_4', to one capacitor voltage level. This limits the voltage stress on the switches and permits the use of switches which are rated fraction of the dc bus voltage. Using V_0 as reference point, there are five switch combinations to synthesize five level voltages across V_j and V_0. Table B.1 lists the voltage levels and their corresponding switch states. State condition 1 means the switch is on, and 0 means the switch is off. The complimentary switch pair means that turning on one of the switches pair will exclude the other from being turned on. With reference to table B.1, it can be seen that the total conduction time per cycle of each switches are not equal. This implies that the current ratings of the switches will be different. However, the voltage ratings can be the same for all switches. Assuming that all switching devices have equal voltage rated, the number of switches needed for an *m*-level single pole MLDC-VSC is

$$N_{switch} = 2(m-1) \qquad \text{(B.1.2)}$$

Although each active switching device is only required to block one capacitor voltage level, this is not the case for the clamping diodes. For example, during synthesis of voltage level V_0, all switches S_1'-S_4' are turned on, clamping diodes D_{1b}-D_{1d} needs to withstand three capacitor voltage levels while D_{2c}-D_{2d} needs to withstand two capacitor voltage levels and so on. In figure B.1(c), clamping diodes are assumed to be equally rated as the active switches and hence the series connection. In general, the diode-clamped topology suffers from the quadratic increase of diode numbers as the number of levels increases. Provided that all the diodes are equally rated and equal to one step level, the number of diodes needed for general *m*-level converters is given as

$$N_{diode} = (m-1)(m-2) \qquad \text{(B.1.3)}$$

Conventionally, when the MLDC-VSC is transferring active powers, the capacitor voltages will drift away from each other due to unequal charge and discharge time. This problem becomes more severe when $m>3$. In order to retain the capacitor voltages at a desired value, the following approaches have been proposed in the technical literatures:

- Use of separate dc sources, one per capacitor. The dc sources are usually provided by a transformer through a rectifier bridge [26 & 36]. This solution is bulky, heavy, inefficient and expensive.
- Use of an auxiliary converter to inject a current in the neutral point of an NPC to balance the dc capacitor voltages [19, 29 & 27]. This leads to additional power hardware which adds to system cost and complexity.
- To provide a current path between the neutral point of the NPC and the neutral point of corresponding ac system [20]. This solution will lead to zero sequence current through the ac side which is unacceptable is most applications.
- To modify the switching patterns accordingly in order to maintain the required capacitor voltages [30, 31 & 35].

The last solution is the most preferred one since it adds very little to system cost and circuit complexity. The drawbacks are the control strategy is made more complex and limitation of converter to low power factor operation.

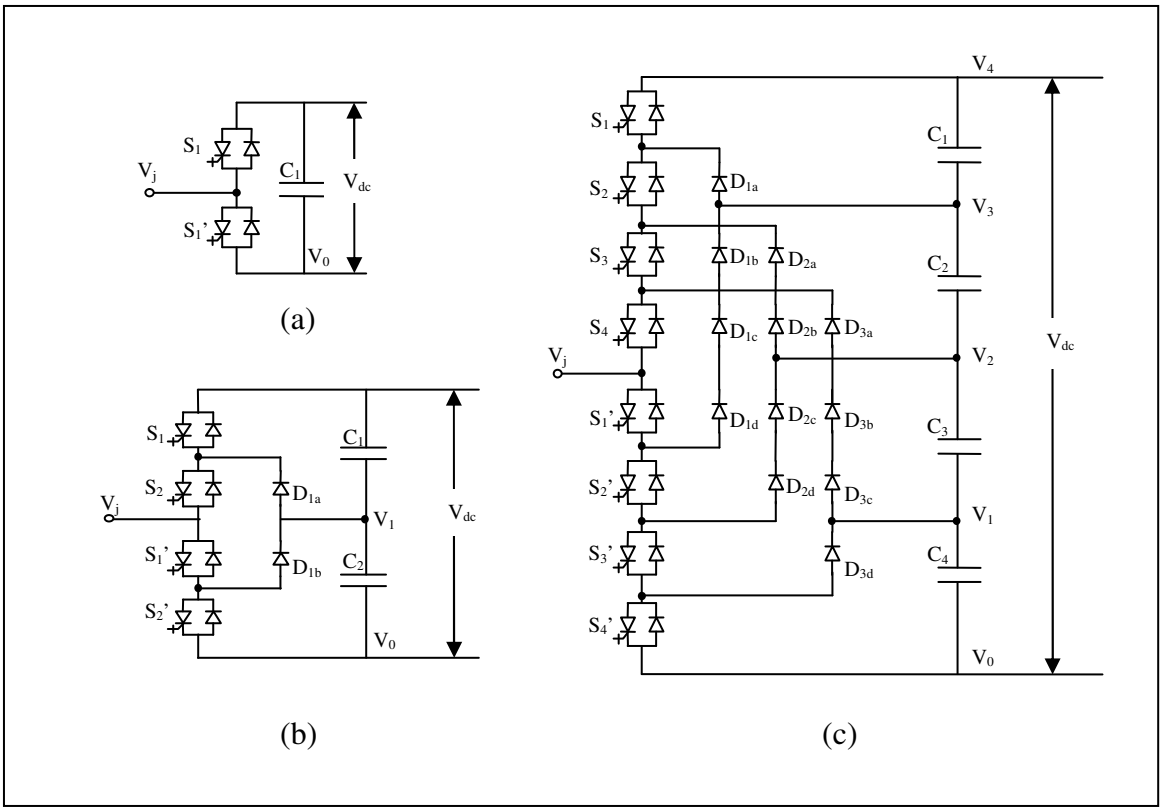


Figure B.1 Diode-clamped multi-level converter
a) two-level topology;
b) three-level topology (also named as Neutral-Point-Clamped);
c) five-level topology.

Table B.1 Voltage levels and their switching states for single pole 5-level MLDC-VSC.

Voltage output V_{j0}	Switch state							
	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$V_4=V_{dc}$	1	1	1	1	0	0	0	0
$V_3=3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_2=V_{dc}/2$	0	0	1	1	1	1	0	0
$V_1=V_{dc}/4$	0	0	0	1	1	1	1	0
$V_0=0$	0	0	0	0	1	1	1	1

B.2 Flying-Capacitor-Clamped Topology

The flying-capacitor-clamped topology uses floating capacitors to form a multi-level voltage divider. Figure B.2 shows the single pole circuit of a multi-level capacitor clamped voltage source converter (MLCC-VSC) from 2 to 5 levels. Assuming that each capacitor has the same voltage ratings, the series connection of capacitors indicates the voltage level between clamping points. Similar to the MLDC-VSC, voltage stress on the switches are clamped to one capacitor voltage level.

The voltage synthesis in a flying-capacitor converter has more flexibility than a MLDC-VSC. Using figure B.2(c) as an example, the voltage of 5 voltage levels can be synthesised by the following combinations:

- For voltage level $V_{j0}=V_{dc}$, turn on all upper switches S_1 to S_4.
- For voltage level $V_{j0}=3V_{dc}/4$, there are four combinations:
  - S_1,S_2,S_3,S_4' ($V_{j0}=V_{dc}-V_{dc}/4$)
  - S_2,S_3,S_4,S_1' ($V_{j0}=3V_{dc}/4$)
  - S_1,S_3,S_4,S_2' ($V_{j0}=V_{dc}-3V_{dc}/4+V_{dc}/2$)
  - S_1,S_2,S_4,S_3' ($V_{j0}=V_{dc}-V_{dc}/2+V_{dc}/4$)
- For voltage level $V_{j0}=V_{dc}/2$, there are six combinations:
  - S_1,S_2,S_3',S_4' ($V_{j0}=V_{dc}-V_{dc}/2$)
  - S_3,S_4,S_1',S_2' ($V_{j0}=V_{dc}/2$)
  - S_1,S_4,S_2',S_3' ($V_{j0}=V_{dc}-3V_{dc}/4+V_{dc}/2-V_{dc}/4$)
  - S_1,S_4,S_2',S_3' ($V_{j0}=V_{dc}-3V_{dc}/4+V_{dc}/4$)
  - S_2,S_4,S_1',S_3' ($V_{j0}=3V_{dc}/4-V_{dc}/2+V_{dc}/4$)
  - S_2,S_3,S_1',S_4' ($V_{j0}=3V_{dc}/4-V_{dc}/4$)
- For voltage level $V_{j0}=V_{dc}/4$, there are four combinations:
  - S_1,S_2',S_3',S_4' ($V_{j0}=V_{dc}-3V_{dc}/4$)
  - S_4,S_1',S_2',S_3' ($V_{j0}=V_{dc}/4$)
  - S_3,S_1',S_2',S_4' ($V_{j0}=V_{dc}/2-V_{dc}/4$)
  - S_2,S_1',S_3',S_4' ($V_{j0}=3V_{dc}/4-V_{dc}/2$)

Table B.2 lists one set of possible combinations to synthesize the 5 voltage levels.

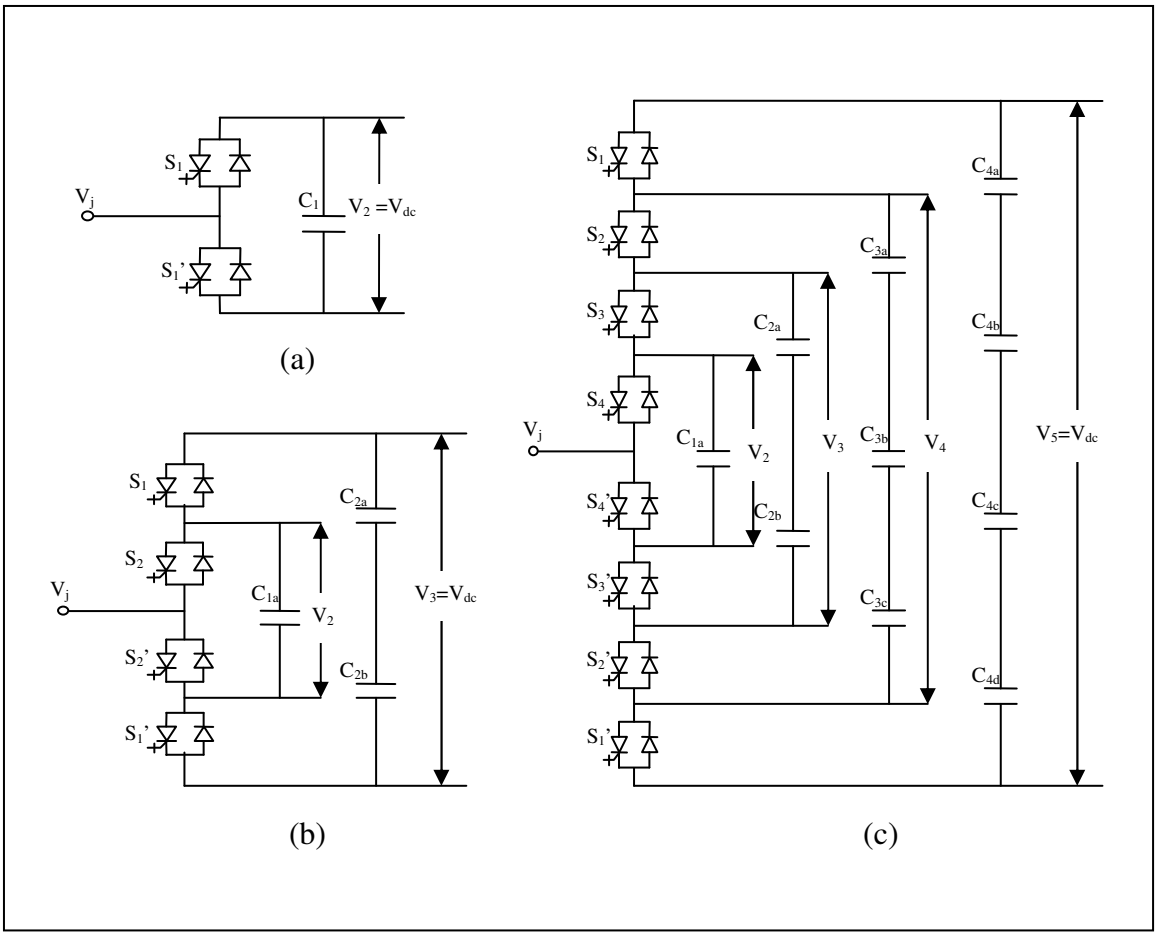


Figure B.2 Flying-capacitor-clamped multi-level converter
a) two-level topology;
b) three-level topology;
c) five-level topology.

Table B.2 Voltage levels and their switching states for single pole 5-level MLCC-VSC.

Voltage output V_{j0}	Switch state							
	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_3=V_{dc}/2$	1	1	0	0	1	1	0	0
$V_2=V_{dc}/4$	1	0	0	0	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

The MLCC-VSC offers greater flexibility in switch state combination to synthesize the intermediate voltage levels, i.e. $3V_{dc}/4$, $V_{dc}/2$ and $V_{dc}/4$ in the case of 5-level MLCC-VSC. Thus, by proper selection of switch combinations, the MLCC-VSC can be used for active power conversion, operation where the MLDC-VSC will encounter capacitor voltage imbalance problem. However, the selection may be very complicated and the switching frequency have to be made higher than the fundamental frequency.

While the number of switches needed in the MLCC-VSC is the same as MLDC-VSC as

$$N_{switch} = 2(m-1), \qquad \text{(B.2.1)}$$

it suffers greatly from the quadratic increase of number of capacitors as *m* increases. This is due to the provision of auxiliary capacitors as compared to only dc bus capacitors in the MLDC-VSC. Provided that all capacitors are of same voltage ratings, the number of capacitors needed for some *m*-level MLCC-VSC is

$$N_{capacitor} = m(m-1)/2 \qquad \text{(B.2.2)}$$

Due to this reason, the MLCC-VSC is not a common candidate for converters despite its synthesis flexibility.

B.3 Generalised bi-Logic Topology

In his attempt to generalise the diode-clamped and flying-capacitor-clamped topologies, Fang [11] had arrived at the proposal for a generalise bi-logic multi-level converter (MLGB-VSC). It offers a solution to the capacitor balancing problem in an MLVSC operating under active power transfer. Figure B.3(a) shows the single pole circuit of MLGB-VSC. The basic building block of this topology is a bi-logic cell, named as P2 cell, which produces two voltage levels of V_{j0}. Note the similarity between the P2 cell, the two-level MLCC-VSC and two-level MLDC-VSC. By connecting some numbers of P2 cell in a pyramid structure, it is possible to build an MLGB-VSC with any level number. An *m*-level MLGB-VSC is obtained by cutting off the *m*-level line in figure B.3(a). For example, a 2-level MLGB-VSC obtained by cutting off at 2-level line.

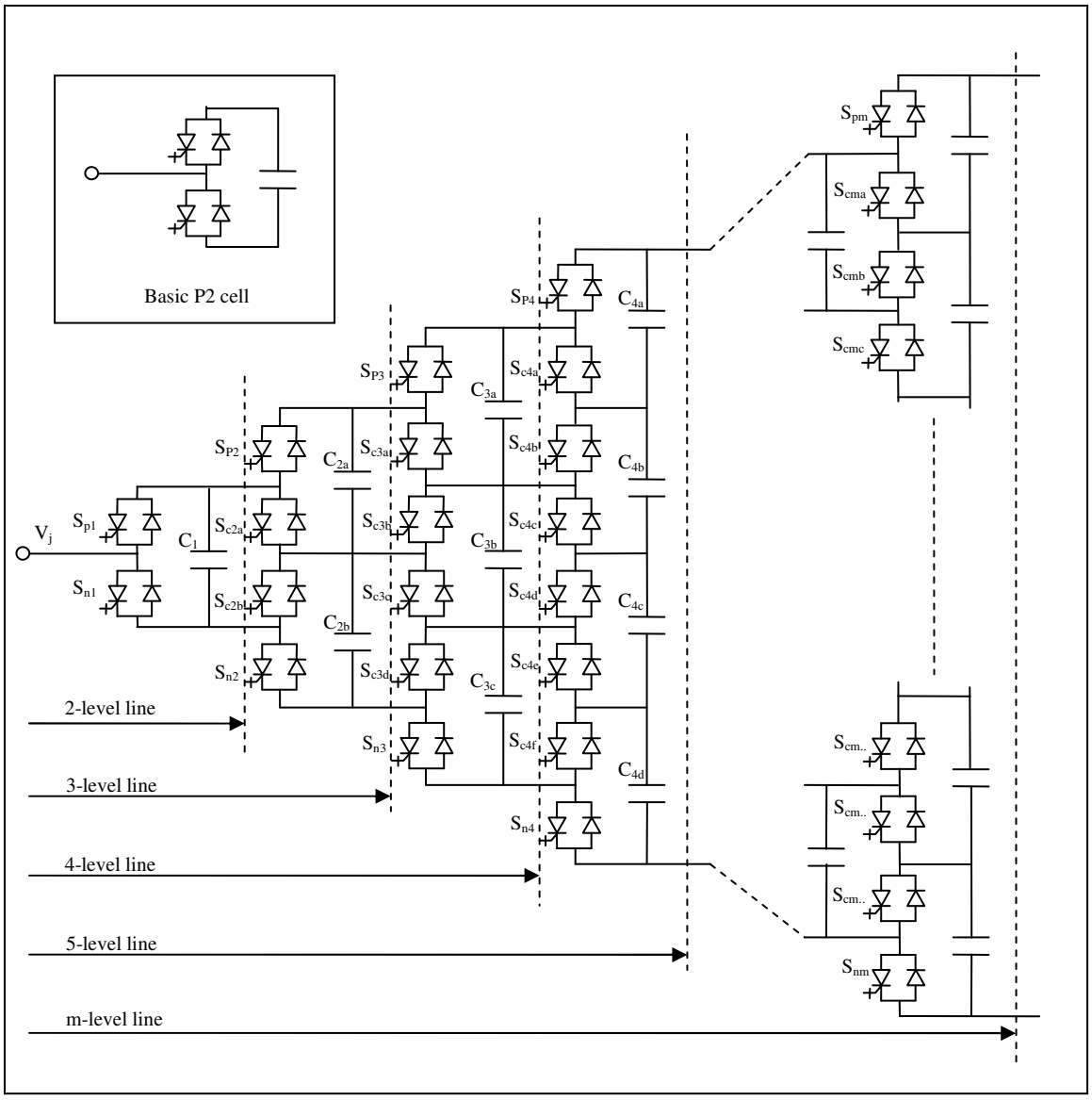


Figure B.3(a) Generalised bi-logic multi-level converter (m-level topology).
Insert: Basic P2 cell

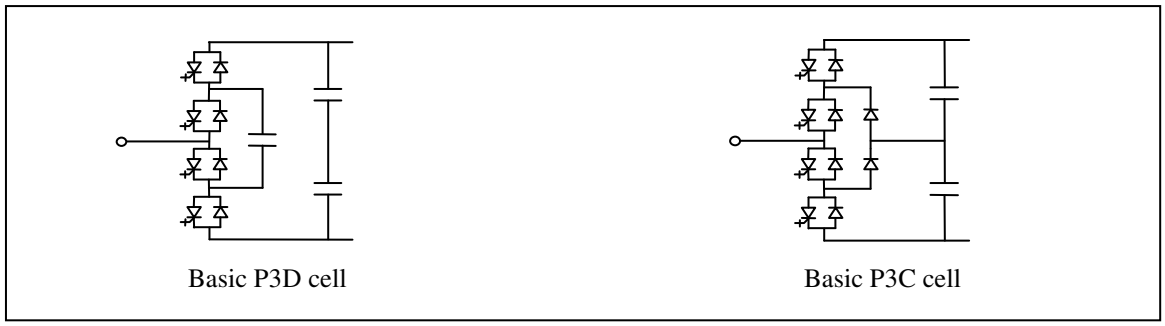


Figure B.3(b) Basic P3 cell.
P3D: tri-logic cell based on diode-clamped topology.
P3C: tri-logic cell based on capacitor-clamped topology.

Table B.3 Voltage levels and their switching states for single pole 5-level MLGB-VSC. Only $S_{p...}$ are shown. The rest of the switch states can be determined from the complimentary rule.

Output Voltage	Capacitor Path*	Switch-state			
		S_{p1}	S_{p2}	S_{p3}	S_{p4}
0V	None	0	0	0	0
$V_{dc}/4$	$+C_1$	1	0	0	0
	$-C_1+C_{2a}+C_{2b}$	0	1	0	0
	$-C_{2b}–C_{2a}+C_{3a}+C_{3b}+C_{3c}$	0	0	1	0
	$-C_{3c}–C_{3b}–C_{3a}+C_{4a}+C_{4b}+C_{4c}+C_{4d}$	0	0	0	1
$V_{dc}/2$	$+C_{2a}+C_{2b}$	1	1	0	0
	$-C_1+C_{3a}+C_{3b}+C_{3c}$	0	1	1	0
	$-C_{2b}-C_{2a}+C_{4a}+C_{4b}+C_{4c}+C_{4d}$	0	0	1	1
	$+C_1-C_{2b}–C_{2a}+C_{3a}+C_{3b}+C_{3c}$	1	0	1	0
	$+C_1-C_{3c}-C_{3b}-C_{3a}+C_{4a}+C_{4b}+C_{4c}+C_{4d}$	1	0	0	1
	$+C_1+C_{2a}+C_{2b}–C_{3c}–C_{3b}–C_{3a}+C_{4a}+C_{4b}+C_{4c}+C_{4d}$	0	1	0	1
$3V_{dc}/4$	$+C_{3a}+C_{3b}+C_{3c}$	1	1	1	0
	$-C_1+C_{4a}+C_{4b}+C_{4c}+C_{4d}$	0	1	1	1
	$+C_{2a}+C_{2b}-C_{3c}-C_{3b}-C_{3a}+C_{4a}+C_{4b}+C_{4c}+C_{4d}$	1	1	0	1
	$+C_1-C_{2b}-C_{2a}+C_{4a}+C_{4b}+C_{4c}+C_{4d}$	1	0	1	1
V_{dc}	$+C_{4a}+C_{4b}+C_{4c}+C_{4d}$	1	1	1	1

* The capacitor path shows those capacitors that are connected to the output for each corresponding switching state. “+” shows that the capacitor is connected positively to the output and “-” shows that the capacitor is connected negatively.

The main switches involved synthesising the *m* voltage levels are those in the outer link, $S_{p...}$ and $S_{n...}$.The rest of the switches $S_{c...}$ are for clamping and balancing purposes. These clamping switches together with their anti-parallel diodes ensure that all capacitor voltages are self-balanced all the time, regardless of the operating condition. Like the MLCC-VSC, there are redundant switch state combinations to synthesise the mid-level voltages. Table B.3 lists the voltage levels and their switch state combinations for a 5-level MLGB-VSC. Only the outer link switches, $S_{p...}$ are shown because the switch states of the $S_{n...}$ and $S_{c...}$ can be determined by following the complimentary rule: if the state of any switch in a column is known, the state of any adjacent two switches are complimentary to it.

Because the basic P2 cell is essentially a 2-level MLDC-VSC or MLCC-VSC, generic MLDC-VSC and MLCC-VSC topology can be deduced from the MLGB-VSC topology**.** By removing all the capacitors except those in the last column and replacing all the clamping switches with blocking diodes, an MLDC-VSC is deduced. Removing all the clamping switches will yield an MLCC-VSC topology.

The main advantage of this topology is the ability to balance capacitor voltage. This is done via the path provided by the clamping switches and that capacitors are connected in parallel to enforce voltage sharing between them. However, this topology is unattractive from the perspective of the number of circuit elements utilised. Both numbers of switches and capacitors are quadratic functions of level number as

$$N_{switch} = m(m-1) \qquad \text{(B.3.1)}$$

$$N_{capacitor} = m(m-1)/2 \qquad \text{(B.3.2)}$$

A way to overcome this problem is to use a tri-logic cell, shown in figure B.3(b), as building block rather than bi-logic. However, the number of circuit elements are still quadratic functions of level number. A basic cell with a logic level higher than 3 is not preferred because, again, it will encounter voltage balancing problem.

B.4 Cascaded H-bridge Topology

This topology was originally intended to connect separated dc sources to the mains to perform either rectifying or inverting operation [18]. It consists of a string of cascaded voltage source converters which are able to synthesize bipolar voltage output. The basic building block is a four-switch connected voltage source converter. Due to its schematic resemblance, it is usually termed as the "H-bridge converter". A string of n cascaded H-bridge converter can produce up to $2n+1$ level of voltage waveform. Figure B.4(a) shows the cascaded H-bridge converter and the ac output waveform for a 9-level H-bridge converter.

Except for the highest and lowest levels, there are many switch state combinations to synthesize a specific level. The flexibility grows as the number of H-bridges increases and the level to be synthesized approaches mid-level. Table B.4 lists the possible switch state combinations to realise the 9-level voltage waveform.

For back-to-back configuration, the string of n cascaded H-bridges has to be duplicated. This is due to the fact that asynchronous operation of the two VSCs will create a short-circuit on the dc bus. The duplicate cascaded string of H-bridges are extended to the upper part of the original string to uphold the dc bus voltage. Voltage output is obtained at the mid-point of this longer string of H-bridge. Figure B.4(b) shows the cascaded H-bridge topology for back-to-back connection. The output voltage levels are obtained by switching in/out of the separate dc source. Although each individual H-bridge can be connected in negative polarity, it should be noted that in the application in MLVR-VSC, the voltage V_j can not be lower than V_o. If this happens, the anti-parallel diode on the main bridge will be forward biased, creating a short-circuit on the main bridge.

The drawback of this topology is the large amount of circuit elements utilised, especially for the back-to-back configuration. While the number of capacitors required is double of that of MLDC-VSC, the number of switches required is four fold. For the purpose of definition conformity with the MLDC-VSC and MLCC-VSC, the level in a cascaded H-bridge based converter is defined as $m=2n+1$. The number of circuit elements required for a m level converter is

$$N_{switch} = 8(m-1) \qquad \text{(B.4.1)}$$

$$N_{capacitor} = 2(m-1) \qquad \text{(B.4.2)}$$

Because the high number of switches used, i.e. 8 times the level number, the conventional cascaded H-bridge converter application for back-to-back VSCs is not favourable.

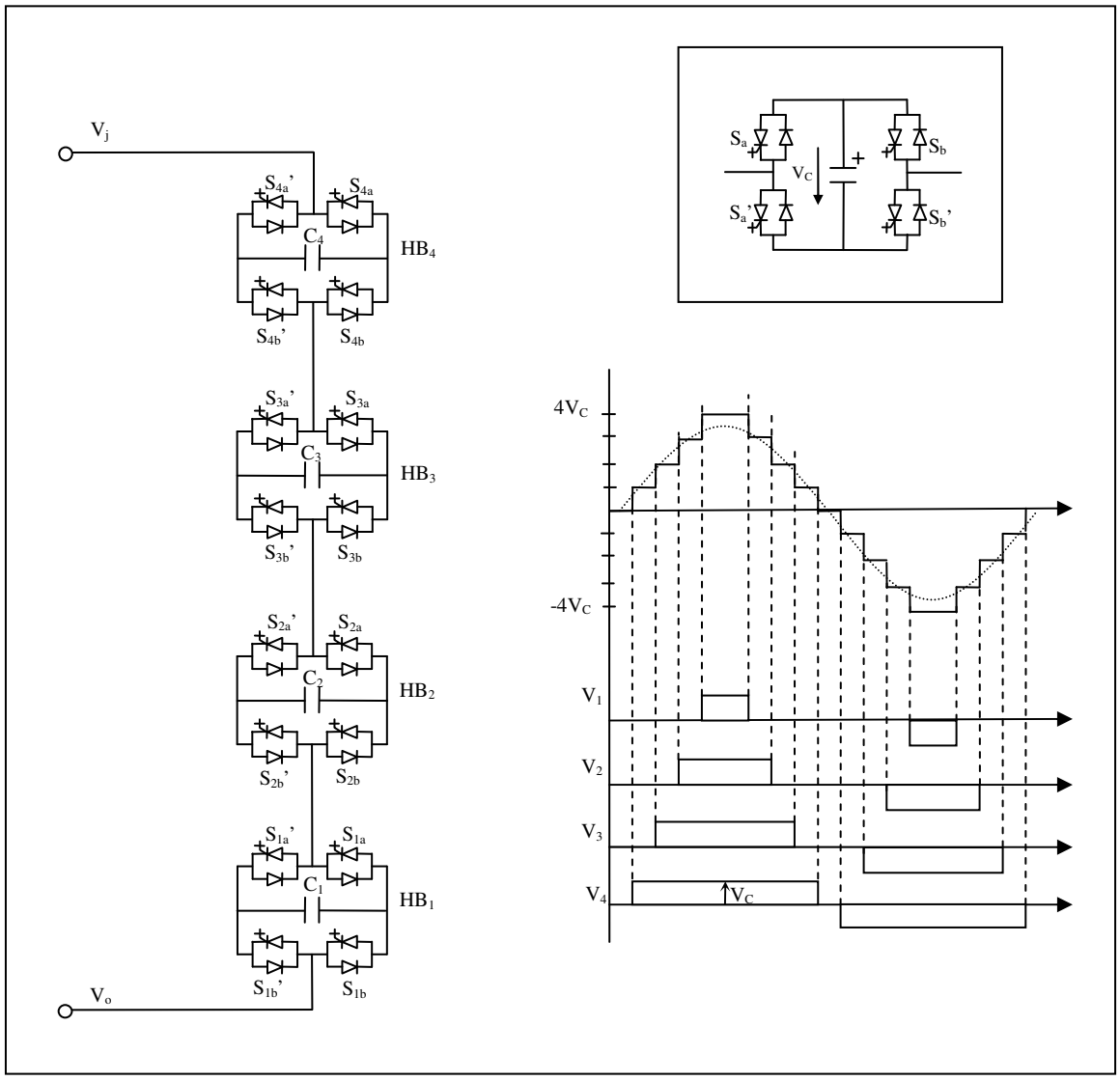


Figure B.4(a) Circuit diagram and the phase voltage waveform of a cascaded H-bridge based converter. Insert: basic building block of a four-switch-connected converter.

Table B.4 Switch states of a 4 cascaded H-bridge (9-level waveform)

Output Voltage, V_{jo}	Capacitor Path*	Switch-state*,**							
		S_{H1a}	S_{H1b}	S_{H2a}	S_{H2b}	S_{H3a}	S_{H3b}	S_{H4a}	S_{H4b}
$4V_C$	$+C_{H1}+C_{H2}+C_{H3}+C_{H4}$	1	0	1	0	1	0	1	0
$3V_C$	$+C_{H1}+C_{H2}+C_{H3}$	1	0	1	0	1	0	1/0	1/0
	$+C_{H1}+C_{H2}+C_{H4}$	1	0	1	0	1/0	1/0	1	0
	$+C_{H1}+C_{H3}+C_{H4}$	1	0	1/0	1/0	1	0	1	0
	$+C_{H2}+C_{H3}+C_{H4}$	1/0	1/0	1	0	1	0	1	0
$2V_C$	$+C_{H1}+C_{H2}$	1	0	1	0	1/0	1/0	1/0	1/0
	$+C_{H1}+C_{H3}$	1	0	1/0	1/0	1	0	1/0	1/0
	$+C_{H1}+C_{H4}$	1	0	1/0	1/0	1/0	1/0	1	0
	$+C_{H2}+C_{H3}$	1/0	1/0	1	0	1	0	1/0	1/0
	$+C_{H2}+C_{H4}$	1/0	1/0	1	0	1/0	1/0	1	0
	$+C_{H3}+C_{H4}$	1/0	1/0	1/0	1/0	1	0	1	0
	$+C_{H1}+C_{H2}+C_{H3}-C_{H4}$	1	0	1	0	1	0	0	1
	$+C_{H1}+C_{H2}-C_{H3}+C_{H4}$	1	0	1	0	0	1	1	0
	$+C_{H1}-C_{H2}+C_{H3}+C_{H4}$	1	0	0	1	1	0	1	0
	$-C_{H1}+C_{H2}+C_{H3}+C_{H4}$	0	1	1	0	1	0	1	0
V_C	$+C_{H1}$	1	0	1/0	1/0	1/0	1/0	1/0	1/0
	$+C_{H2}$	1/0	1/0	1	0	1/0	1/0	1/0	1/0
	$+C_{H3}$	1/0	1/0	1/0	1/0	1	0	1/0	1/0
	$+C_{H4}$	1/0	1/0	1/0	1/0	1/0	1/0	1	0
	$+C_{H1}+C_{H2}-C_{H3}$	1	0	1	0	0	1	1/0	1/0
	$+C_{H1}-C_{H2}+C_{H3}$	1	0	0	1	1	0	1/0	1/0
	$-C_{H1}+C_{H2}+C_{H3}$	0	1	1	0	1	0	1/0	1/0
	$+C_{H1}+C_{H2}-C_{H4}$	1	0	1	0	1/0	1/0	0	1
	$+C_{H1}-C_{H2}+C_{H4}$	1	0	0	1	1/0	1/0	1	0
	$-C_{H1}+C_{H2}+C_{H4}$	0	1	1	0	1/0	1/0	1	0
	$+C_{H1}+C_{H3}-C_{H4}$	1	0	1/0	1/0	1	0	0	1
	$+C_{H1}-C_{H3}+C_{H4}$	1	0	1/0	1/0		1	1	0
	$-C_{H1}+C_{H3}+C_{H4}$	0	1	1/0	1/0	1	0	1	0
	$+C_{H2}+C_{H3}-C_{H4}$	1/0	1/0	1	0	1	0	0	1
	$+C_{H2}-C_{H3}+C_{H4}$	1/0	1/0	1	0	0	1	1	0
	$-C_{H2}+C_{H3}+C_{H4}$	1/0	1/0	0	1	1	0	1	0
0	None	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
	$+C_{H1}-C_{H2}$	1	0	0	1	1/0	1/0	1/0	1/0
	$+C_{H1}-C_{H3}$	1	0	1/0	1/0	0	1	1/0	1/0
	$+C_{H1}-C_{H4}$	1	0	1/0	1/0	1/0	1/0	0	1
	$-C_{H1}+C_{H2}$	0	1	1	0	1/0	1/0	1/0	1/0
	$-C_{H1}+C_{H3}$	0	1	1/0	1/0	1	0	1/0	1/0
	$-C_{H1}+C_{H4}$	0	1	1/0	1/0	1/0	1/0	1	0
	$+C_{H2}-C_{H3}$	1/0	1/0	1	0	0	1	1/0	1/0
	$+C_{H2}-C_{H4}$	1/0	1/0	1	0	1/0	1/0	0	1
	$-C_{H2}+C_{H3}$	1/0	1/0	0	1	1	0	1/0	1/0
	$-C_{H2}+C_{H4}$	1/0	1/0	0	1	1/0	1/0	1	0
	$+C_{H3}-C_{H4}$	1/0	1/0	1/0	1/0	1	0	0	1
	$-C_{H3}+C_{H4}$	1/0	1/0	1/0	1/0	0	1	1	0
	$+C_{H1}+C_{H2}-C_{H3}-C_{H4}$	1	0	1	0	0	1	0	1
	$+C_{H1}-C_{H2}+C_{H3}-C_{H4}$	1	0	0	1	1	0	0	1
	$+C_{H1}-C_{H2}-C_{H3}+C_{H4}$	1	0	0	1	0	1	1	0
	$-C_{H1}+C_{H2}+C_{H3}-C_{H4}$	0	1	1	0	1	0	0	1
	$-C_{H1}+C_{H2}-C_{H3}+C_{H4}$	0	1	1	0	0	1	1	0
	$-C_{H1}-C_{H2}+C_{H3}+C_{H4}$	0	1	0	1	1	0	1	0

$-V_C$	$-C_{H1}$	0	1	1/0	1/0	1/0	1/0	1/0	1/0
	$-C_{H2}$	1/0	1/0	0	1	1/0	1/0	1/0	1/0
	$-C_{H3}$	1/0	1/0	1/0	1/0	0	1	1/0	1/0
	$-C_{H4}$	1/0	1/0	1/0	1/0	1/0	1/0	0	1
	$-C_{H1}-C_{H2}+C_{H3}$	0	1	0	1	1	0	1/0	1/0
	$-C_{H1}+C_{H2}-C_{H3}$	0	1	1	0	0	1	1/0	1/0
	$+C_{H1}-C_{H2}-C_{H3}$	1	0	0	1	0	0	1/0	1/0
	$-C_{H1}-C_{H2}+C_{H4}$	0	1	0	1	1/0	1/0	1	0
	$-C_{H1}+C_{H2}-C_{H4}$	0	1	1	0	1/0	1/0	0	1
	$+C_{H1}-C_{H2}-C_{H4}$	1	0	0	1	1/0	1/0	0	1
	$-C_{H1}-C_{H3}+C_{H4}$	0	1	1/0	1/0	0	1	1	0
	$-C_{H1}+C_{H3}-C_{H4}$	0	1	1/0	1/0	1	0	0	1
	$+C_{H1}-C_{H3}-C_{H4}$	1	0	1/0	1/0	0	1	0	1
	$-C_{H2}-C_{H3}+C_{H4}$	1/0	1/0	0	1	0	1	1	0
	$-C_{H2}+C_{H3}-C_{H4}$	1/0	1/0	0	1	1	0	0	1
	$+C_{H2}-C_{H3}-C_{H4}$	1/0	1/0	1	0	0	1	0	1
$-2V_C$	$-C_{H1}-C_{H2}$	0	1	0	1	1/0	1/0	1/0	1/0
	$-C_{H1}-C_{H3}$	0	1	1/0	1/0	0	1	1/0	1/0
	$-C_{H1}-C_{H4}$	0	1	1/0	1/0	1/0	1/0	0	1
	$-C_{H2}-C_{H3}$	1/0	1/0	0	1	0	1	1/0	1/0
	$-C_{H2}-C_{H4}$	1/0	1/0	0	1	1/0	1/0	0	1
	$-C_{H3}-C_{H4}$	1/0	1/0	1/0	1/0	0	1	0	1
	$-C_{H1}-C_{H2}-C_{H3}+C_{H4}$	0	1	0	1	0	1	1	0
	$-C_{H1}-C_{H2}+C_{H3}-C_{H4}$	0	1	0	1	1	0	0	1
	$-C_{H1}+C_{H2}-C_{H3}-C_{H4}$	0	1	1	0	0	1	0	1
	$+C_{H1}-C_{H2}-C_{H3}-C_{H4}$	1	0	0	1	0	1	0	1
$-3V_C$	$-C_{H1}-C_{H2}-C_{H3}$	0	1	0	1	0	1	1/0	1/0
	$-C_{H1}-C_{H2}-C_{H4}$	0	1	0	1	1/0	1/0	0	1
	$-C_{H1}-C_{H3}-C_{H4}$	0	1	1/0	1/0	0	1	0	1
	$-C_{H2}-C_{H3}-C_{H4}$	1/0	1/0	0	1	0	1	0	1
$-4V_C$	$-C_{H1}-C_{H2}-C_{H3}-C_{H4}$	0	1	0	1	0	1	0	1

*Only two valves of each H-bridge are shown. The states of the adjacent switches can be determined from the complimentary rule.

**Switch state 1/0 implies that H-bridge is bypassed. During this state, the switch can either be on or off but the state of the switch pair must be the same, i.e. if $S_{Hna}=1$ then $S_{Hnb}=1$ or if $S_{Hna}=0$ then $S_{Hnb}=0$.

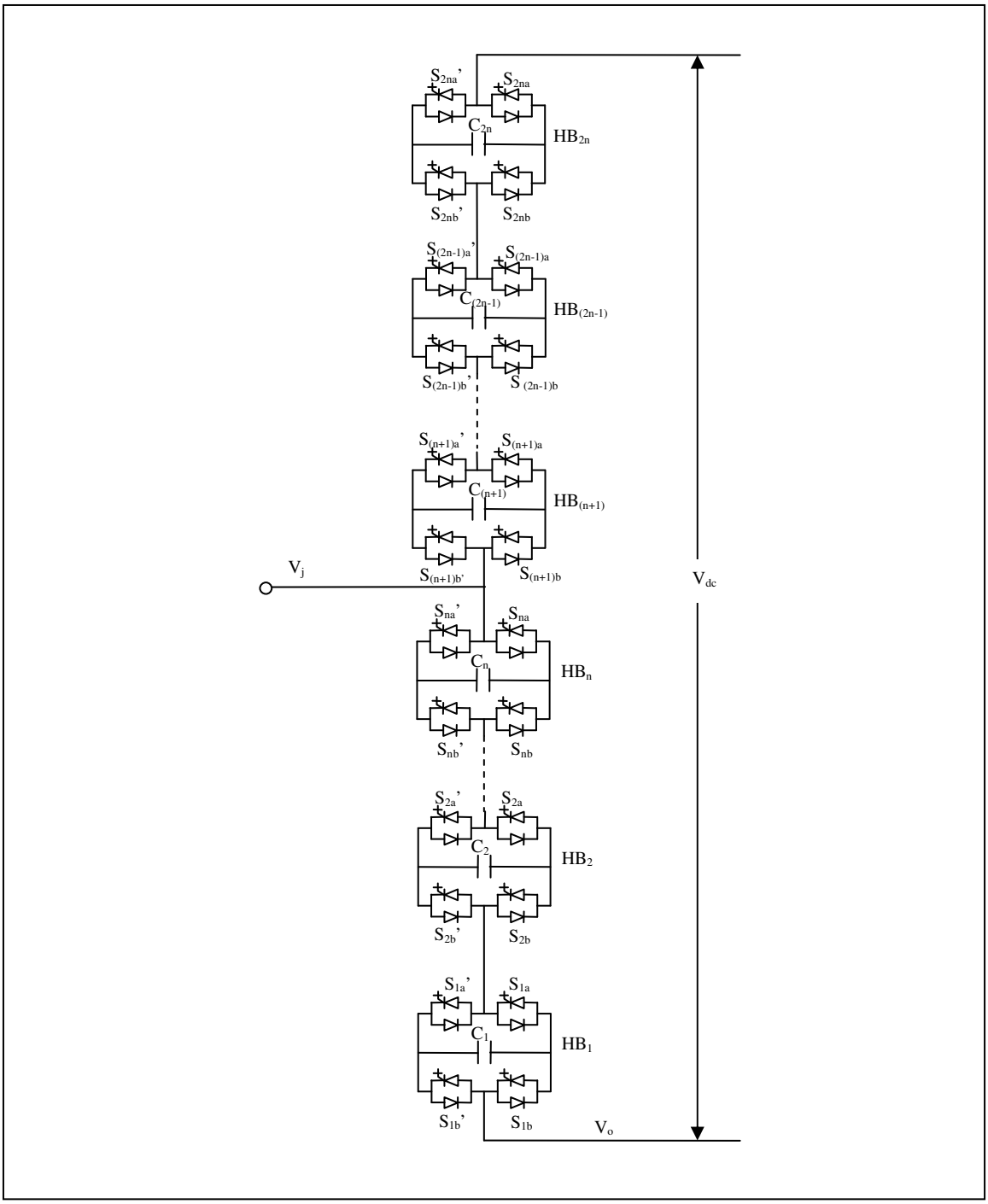


Figure B.4(b) Cascaded H-bridge multi-level converter for back-to-back VSCs configuration.

APPENDIX C

Mathematical Evaluation of MLVR-VSC Harmonic Analysis

C.1 Voltage Waveform Analysis

The MLVR-VSC output voltage analysis is performed with the following assumptions:

- The MLVR-VSC is operating in perfect three phase balance;
- The dc side capacitors of the MLVR-VSC are infinite and the current spike limiting inductor on the reinjection branch is negligibly small compared to the interface transformer leakage reactance. Hence, the output voltage waveform can be assume to contain only characteristics harmonics.

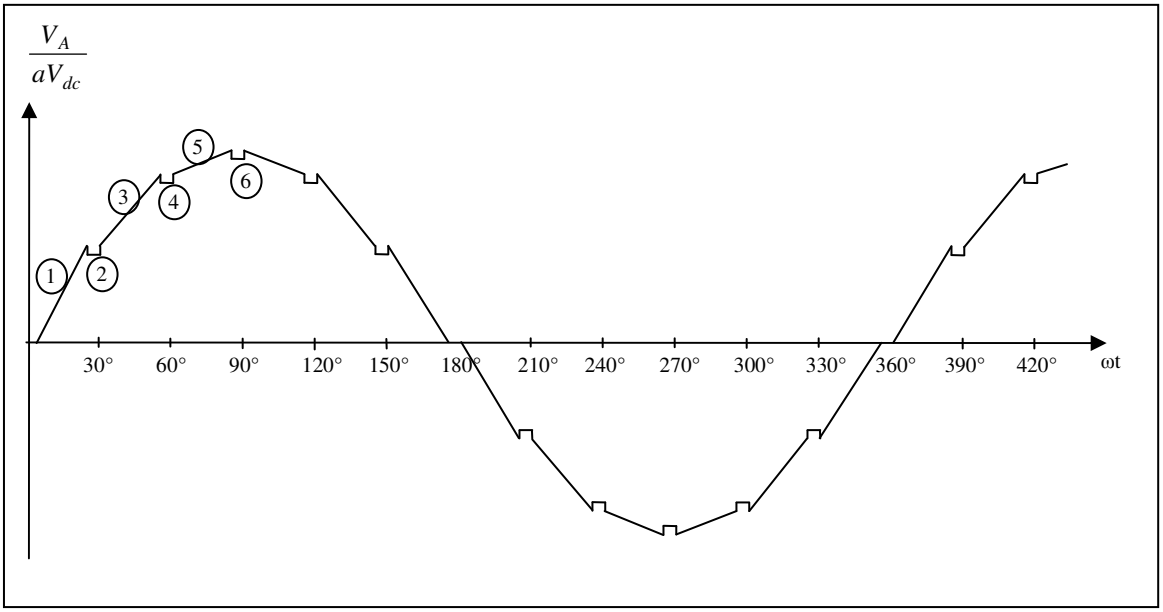


Figure C.1 MLVR-VSC phase A output voltage waveform (modulated).

Figure C.1 shows the phase A output voltage waveform (normalised to transformed dc bus voltage, aV_{dc}) of an ideal MLVR-VSC with modulation. Since the waveform is quarterwave symmetry, it can be sufficiently described with a partial continuous function from ωt=0° up to ωt=90°. This partial continuous function is given as

$$f_V(\omega t)=\begin{cases}0 & for \quad 0\le \omega t\le W/2;\\ \frac{1}{3}\left(\frac{t}{\pi/6-w}-\frac{w/2}{\pi/6-w}\right) & for \quad W/2\le \omega t\le \pi/6-W/2;\\ \frac{1}{3}\left(1-\frac{d}{100}\right) & for \quad \pi/6-W/2\le \omega t\le \pi/6+W/2;\\ \frac{t}{\pi/6-w}\left(\frac{1}{\sqrt{3}}-\frac{1}{3}\right)+\frac{\pi/3-w/2-\sqrt{3}(\pi/6+w/2)}{3(\pi/6-w)} & for \quad \pi/6+w/2\le \omega t\le \pi/3-W/2;\\ \frac{1}{\sqrt{3}}\left(1-\frac{d}{100}\right) & for \quad \pi/3-W/2\le \omega t\le \pi/3+W/2;\\ \frac{t}{\pi/6-w}\left(\frac{2}{3}-\frac{1}{\sqrt{3}}\right)+\frac{2}{3}\left(\frac{\sqrt{3}/2(\pi/2-w/2)-\pi/3-w/2}{\pi/6-w}\right) & for \quad \pi/3+W/2\le \omega t\le \pi/2-W/2;\\ \frac{2}{3}\left(1-\frac{d}{100}\right) & for \quad \pi/2-W/2\le \omega t\le \pi/2.\end{cases}$$

(C.1.1)

The Fourier analysis of the waveform in figure C.1 only consists of sine terms given as

$$\frac{V_{An}}{aV_{dc}}=\frac{8}{3n\pi}\left\{\frac{2\sin n\left(\frac{\pi}{12}-\frac{W}{2}\right)\cos\frac{n\pi}{6}\cos\frac{n\pi}{12}}{n^2\left(\frac{\pi}{6}-W\right)}\left[4\sqrt{3}-7-4\left(\sqrt{3}-2\right)\cos^2\frac{n\pi}{12}\right]-f_{Vn}(d,W)\right\}$$

(C.1.2)

Where

a = transformation ratio of interface transformer

V_{dc} = dc bus voltage

d = modulation notch depth on the dc side waveform

W = modulation notch width on the dc side waveform

$$f_{Vn}(d,W)=\frac{d}{100}\sin\frac{nW}{2}\sin\frac{n\pi}{3}\left(2\cos\frac{n\pi}{6}+\sqrt{3}\right) \qquad \text{(C.1.3)}$$

$n=1,12x\pm1 \qquad for\ x=1,2,3...$

The rms value of the waveform is

$$\frac{V_{Arms}}{aV_{dc}} = \sqrt{\frac{2}{9\pi}\left\{\frac{\left(4+\sqrt{3}\right)\pi}{6} + W\left[6\left(1-\frac{d}{100}\right)^{2} - 4 - \sqrt{3}\right]\right\}} \qquad \text{(C.1.4)}$$

The THD of a waveform is defined as the ratio of the rms of the harmonic content to the rms value of the fundamental quantity, expressed as a percent of the fundamental [16]. Since the V_{Arms} shown in equation C.1.4 contains both the fundamental component and harmonic components, the voltage THD can be calculated as

$$THD_V = \left(\sqrt{\frac{2V_{Arms}^{2}}{V_{A1}^{2}} - 1}\right) \times 100\% \qquad \text{(C.1.5)}$$

C.2 Current Waveform Analysis

The MLVR-VSC output current analysis is performed based on following assumptions:

- The power system at which the MLVR-VSC is connected to is ideal three phase with minimal internal impedance. Hence it can be represented as ideal sinusoidal three phase voltage source, V_S.
- The dc side capacitors of the MLVR-VSC are infinite, hence the MLVR-VSC appear as voltage sources, V_A, V_B and V_C, with harmonics but no internal impedance.
- The interface transformers used to couple the MLVR-VSC output voltage to the power system are equal and their leakage reactances, X_l, only consist of a self term without any mutual coupling between phases.
- The interface transformers are ideal without losses of any kind (core and copper).
- The power system voltage is displaced from the MLVR-VSC output voltage fundamental component by angle of ϕ.

The MLVR-VSC connected to an ideal power system can be modelled as in figure C.2

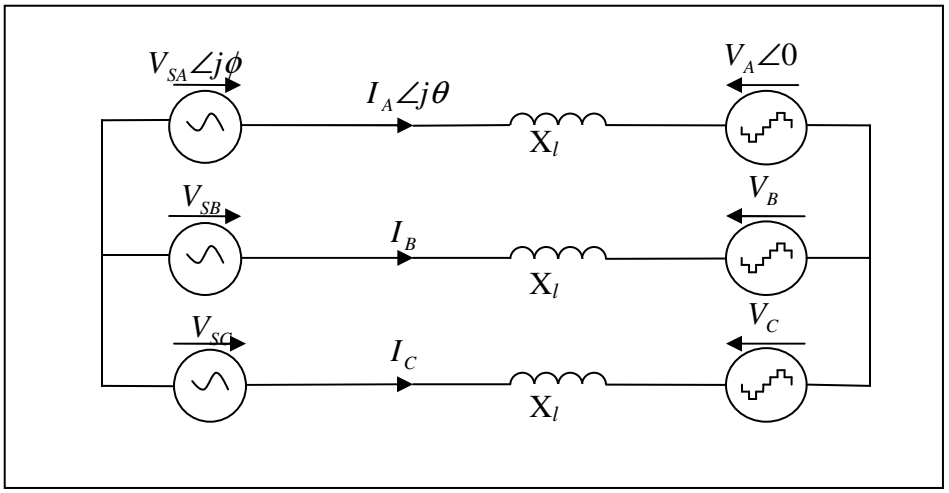


Figure C.2 The simplified model of the MLVR-VSC connected to ideal power system.

The output current, I_o, are caused by linear interaction between the ideal voltage source and the MLVR-VSC voltage source. Hence it can be obtained by superpositioning the current components caused by the voltage sources respectively. The output current vector can be expressed as

$$I_o(\omega t) = F_S(\omega t) - F_o(\omega t) \qquad \text{(C.2.1)}$$

Where

$$I_o(\omega t) = \begin{bmatrix} I_A(\omega t) \\ I_B(\omega t) \\ I_C(\omega t) \end{bmatrix}$$

$$F_o(\omega t) = \begin{bmatrix} f_A(\omega t) \\ f_B(\omega t) \\ f_C(\omega t) \end{bmatrix} \qquad F_S(\omega t) = \frac{V_{Sm}}{X_l} \begin{bmatrix} \cos(\omega t + \phi) \\ \cos(\omega t + \phi - 120°) \\ \cos(\omega t + \phi + 120°) \end{bmatrix}$$

V_{Sm} is the amplitude of the voltage source V_S. The component $F_o(\omega t)$ in equation C.2.1 is the output current caused by MLVR-VSC output voltage and shorting V_S while the component $F_S(\omega t)$ in equation C.2.1 is the output current caused by V_S and shorting MLVR-VSC output voltage. Since the system is assumed to be perfectly three phase balance, analysis on one phase is sufficient to describe the MLVR-VSC output current. The component $f_A(\omega t)$ is given as

$$f_A(\omega t)=\left[\frac{1}{2X_l}\int_0^{\pi}V_A(\omega t)d\omega t-\int_0^{\omega t}\frac{V_A(\omega t)}{X_l}d\omega t\right] \tag{C.2.2}$$

The first part of $f_A(\omega t)$ is given by

$$\begin{aligned}\frac{1}{2X_l}\int_0^{\pi}V_A(\omega t)d\omega t=\frac{aV_{dc}}{X_l}\Bigg[&\int_0^{\frac{W}{2}}0\cdot d\omega t+\int_{\frac{W}{2}}^{\frac{\pi}{6}-\frac{W}{2}}\left\{\frac{1}{3}\left(\frac{t}{\pi/6-w}-\frac{w/2}{\pi/6-w}\right)\right\}\cdot d\omega t\\&+\int_{\frac{\pi}{6}-\frac{W}{2}}^{\frac{\pi}{6}+\frac{W}{2}}\left\{\frac{1}{3}\left(1-\frac{d}{100}\right)\right\}\cdot d\omega t\\&+\int_{\frac{\pi}{6}+\frac{W}{2}}^{\frac{\pi}{3}-\frac{W}{2}}\left\{\frac{t}{\pi/6-w}\left(\frac{1}{\sqrt{3}}-\frac{1}{3}\right)+\frac{\pi/3-w/2-\sqrt{3}(\pi/6+w/2)}{3(\pi/6-w)}\right\}\cdot d\omega t\\&+\int_{\frac{\pi}{3}-\frac{W}{2}}^{\frac{\pi}{3}+\frac{W}{2}}\left\{\frac{1}{\sqrt{3}}\left(1-\frac{d}{100}\right)\right\}\cdot d\omega t\\&+\int_{\frac{\pi}{3}+\frac{W}{2}}^{\frac{\pi}{2}-\frac{W}{2}}\left\{\frac{t}{\pi/6-w}\left(\frac{2}{3}-\frac{1}{\sqrt{3}}\right)+\frac{2}{3}\left(\frac{\sqrt{3}/2(\pi/2-w/2)-\pi/3-w/2}{\pi/6-w}\right)\right\}\cdot d\omega t\\&+\int_{\frac{\pi}{2}-\frac{W}{2}}^{\frac{\pi}{2}}\left\{\frac{2}{3}\left(1-\frac{d}{100}\right)\right\}\cdot d\omega t\Bigg]\\=\frac{aU_{dc}}{X_l}&\left\{\left(\frac{\pi}{6}-W\right)\left(\frac{2+\sqrt{3}}{3}\right)+\frac{W\left(1-\frac{d}{100}\right)}{3}\left(2+\sqrt{3}\right)\right\}\end{aligned} \tag{C.2.3}$$

The second part of $f_A(\omega t)$ is derived based on equation C.1.1, it is given by

$$\int_0^{\omega t}\frac{V_A(\omega t)}{X_l}d\omega t=\frac{aU_{dc}}{X_l}\begin{cases}
0 & for \quad 0<\omega t<\frac{W}{2};\\
\frac{(\omega t-W/2)^2}{6(\pi/6-W)} & for \quad \frac{W}{2}<\omega t<\frac{\pi}{6}-\frac{W}{2};\\
\frac{(1-d/100)}{3}(\omega t-\pi/6+W/2)+\frac{\pi/6-W}{6} & for \quad \frac{\pi}{6}-\frac{W}{2}<\omega t<\frac{\pi}{6}+\frac{W}{2};;\\
\frac{\sqrt{3}-1}{6(\pi/6-W)}(\omega t-\pi/6-W/2)^2+\frac{\omega t-\pi/6-W/2}{3}+\frac{W(1-d/100)}{3}+\frac{\pi/6-W}{6} & for \quad \frac{\pi}{6}+\frac{W}{2}<\omega t<\frac{\pi}{3}-\frac{W}{2};\\
\frac{(1-d/100)}{\sqrt{3}}(\omega t-\pi/3+W/2)+(\pi/6-W)\left(\frac{\sqrt{3}+2}{6}\right)+\frac{W(1-d/100)}{3} & for \quad \frac{\pi}{3}-\frac{W}{2}<\omega t<\frac{\pi}{3}+\frac{W}{2};\\
\frac{2-\sqrt{3}}{6(\pi/6-W)}(\omega t-\pi/3-W/2)^2+\frac{\omega t-\pi/3-W/2}{\sqrt{3}}+\frac{W(1-d/100)(1+\sqrt{3})}{3}+(\pi/6-W)\left(\frac{\sqrt{3}+2}{6}\right) & for \quad \frac{\pi}{3}+\frac{W}{2}<\omega t<\frac{\pi}{2}-\frac{W}{2};\\
\frac{2(1-d/100)}{3}(\omega t-\pi/2+W/2)+(\pi/6-W)\left(\frac{2+\sqrt{3}}{3}\right)+\frac{W(1-d/100)(1+\sqrt{3})}{3} & for \quad \frac{\pi}{2}-\frac{W}{2}<\omega t<\frac{\pi}{2}+\frac{W}{2};\\
\frac{\sqrt{3}-2}{6(\pi/6-W)}(\omega t-\pi/2-W/2)^2+\frac{2}{3}(\omega t-\pi/2-W/2)+(\pi/6-W)\left(\frac{2+\sqrt{3}}{3}\right)+\frac{W(1-d/100)(3+\sqrt{3})}{3} & for \quad \frac{\pi}{2}+\frac{W}{2}<\omega t<\frac{2\pi}{3}-\frac{W}{2};\\
\frac{(1-d/100)}{\sqrt{3}}(\omega t-2\pi/3+W/2)+(\pi/6-W)\left(\frac{2+\sqrt{3}}{3}\right)+\frac{W(1-d/100)(3+\sqrt{3})}{3} & for \quad \frac{2\pi}{3}-\frac{W}{2}<\omega t<\frac{2\pi}{3}+\frac{W}{2};\\
\frac{1-\sqrt{3}}{6(\pi/6-W)}(\omega t-2\pi/3-W/2)^2+\frac{(\omega t-2\pi/3-W/2)}{\sqrt{3}}+(\pi/6-W)\left(\frac{2+\sqrt{3}}{2}\right)+\frac{W(1-d/100)(3+2\sqrt{3})}{3} & for \quad \frac{2\pi}{3}+\frac{W}{2}<\omega t<\frac{5\pi}{6}-\frac{W}{2};\\
\frac{(1-d/100)}{3}(\omega t-5\pi/6+W/2)+(\pi/6-W)\left(\frac{7+4\sqrt{3}}{6}\right)+\frac{W(1-d/100)(3+2\sqrt{3})}{3} & for \quad \frac{5\pi}{6}-\frac{W}{2}<\omega t<\frac{5\pi}{6}+\frac{W}{2};\\
\frac{-(\omega t-5\pi/6-W/2)^2}{6(\pi/6-W)}+\frac{(\omega t-5\pi/6-W/2)}{3}+(\pi/6-W)\left(\frac{7+4\sqrt{3}}{6}\right)+\frac{W(1-d/100)(4+2\sqrt{3})}{3} & for \quad \frac{5\pi}{6}+\frac{W}{2}<\omega t<\pi-\frac{W}{2};\\
(\pi/6-W)\left(\frac{4+2\sqrt{3}}{3}\right)+\frac{W(1-d/100)(4+2\sqrt{3})}{3} & for \quad \pi-\frac{W}{2}<\omega t<\pi.
\end{cases}$$

(C.2.4)

The output current rms value, I_{Arms} can be derived from

$$I_{Arms} = \sqrt{I_{A1rms}^2 + \frac{1}{2\pi}\int_0^{2\pi} f_A^2(\omega t) - \frac{V_{A1}^2}{2X_l^2}} \tag{C.2.5}$$

Where

$$I_{A1rms} = \frac{V_{A1}}{\sqrt{2}X_l}\sqrt{1 + \frac{V_{Sm}^2}{V_{A1}^2} - 2\frac{V_{Sm}}{V_{A1}}\cos\phi} = \frac{V_{A1}}{\sqrt{2}X_l}k \tag{C.2.6}$$

and

$$\begin{aligned}\frac{1}{2\pi}\int_0^{2\pi} f_A^2(\omega t) = \frac{2a^2V_{dc}^2}{\pi X_l^2}\Bigg\{&\left(\frac{\pi}{6} - W\right)^3\left(\frac{636 + 357\sqrt{3}}{540}\right)\\ &+ W\left(\frac{\pi}{6} - W\right)^2\left[\frac{65 + 36\sqrt{3}}{18} - \frac{d}{100}\left(\frac{22 + 12\sqrt{3}}{9}\right)\right]\\ &+ W^2\left(\frac{\pi}{6} - W\right)\left(1 - \frac{d}{100}\right)\left[\frac{11 + 6\sqrt{3}}{3} - \frac{d}{100}\left(\frac{4 + 2\sqrt{3}}{3}\right)\right]\\ &+ W^3\left(1 - \frac{d}{100}\right)^2\left(\frac{11 + 6\sqrt{3}}{9}\right)\Bigg\}\end{aligned} \tag{C.2.7}$$

Alternatively, the rms current can be simplified as

$$I_{Arms} = \frac{V_{A1}}{\sqrt{2}X_l}\sqrt{k^2 + P(d,W) - 1} \tag{C.2.8}$$

Where

$$\begin{aligned}P(d,W) &= \frac{\left(2X_l^2\right)\left[\frac{1}{2\pi}\int_0^{2\pi} f_A^2(\omega t)\right]}{V_{A1}^2}\\ &= \frac{4f_I(d,W)}{\pi\left[\frac{8\sqrt{2-\sqrt{3}}}{\pi(\pi/6 - W)}\sin\left(\frac{\pi}{12} - \frac{W}{2}\right) - \frac{2d}{25\pi}\sin\frac{W}{2}\right]^2}\end{aligned} \tag{C.2.9}$$

Where

$$f_I(d,W)=\left(\frac{\pi}{6}-W\right)^3\left(\frac{636+357\sqrt{3}}{540}\right)+W\left(\frac{\pi}{6}-W\right)^2\left[\frac{65+36\sqrt{3}}{18}-\frac{d}{100}\left(\frac{22+12\sqrt{3}}{9}\right)\right]$$
$$+W^2\left(\frac{\pi}{6}-W\right)\left(1-\frac{d}{100}\right)\left[\frac{11+6\sqrt{3}}{3}-\frac{d}{100}\left(\frac{4+2\sqrt{3}}{3}\right)\right]+W^3\left(1-\frac{d}{100}\right)^2\left(\frac{11+6\sqrt{3}}{9}\right) \quad \text{(C.2.10)}$$

Finally, the THD of the output current becomes

$$\begin{aligned} THD_I &= \sqrt{\frac{I_{Arms}^2}{I_{A1rms}^2}-1}\times 100\% \\ &= \sqrt{\frac{k^2+P(d,W)-1}{k^2}-1}\times 100\% \\ &= \frac{\sqrt{P(d,W)-1}}{k}\times 100\% \end{aligned} \quad \text{(C.2.11)}$$

APPENDIX D: MLVR-VSC Harmonic Spectrums

D.1 Ideal Waveforms (infinite quantisation)

D.1.1 Voltage Harmonics

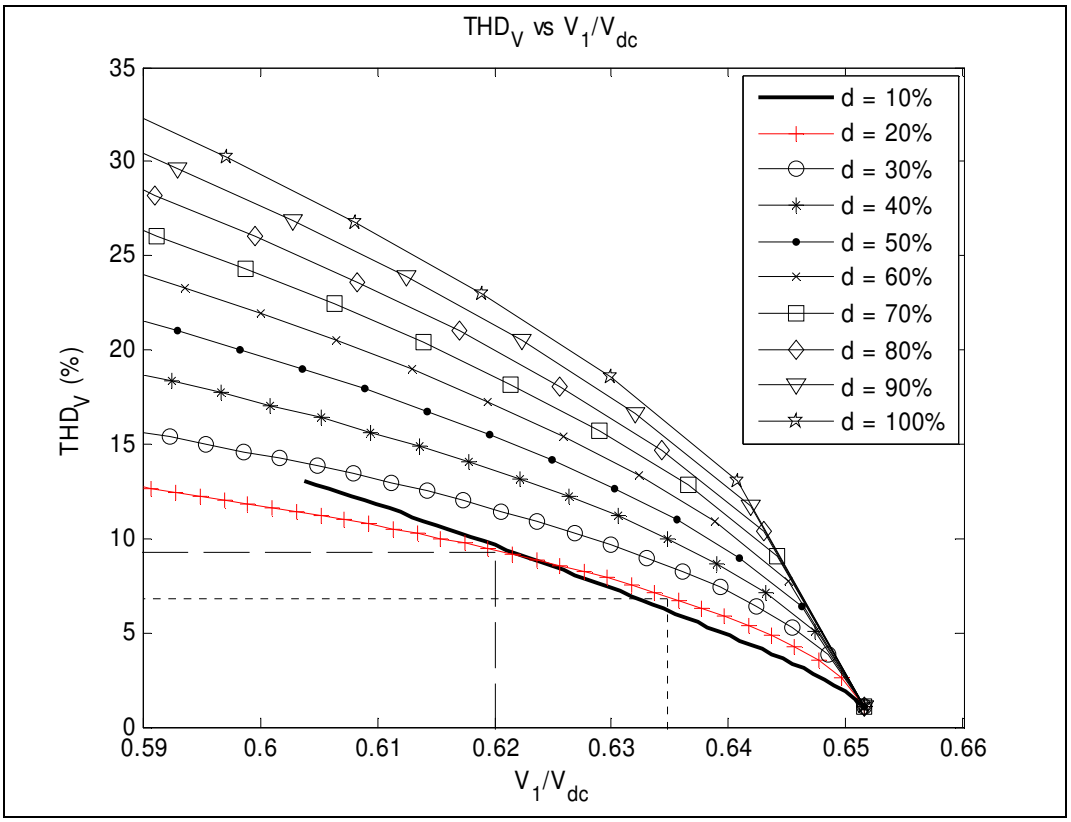
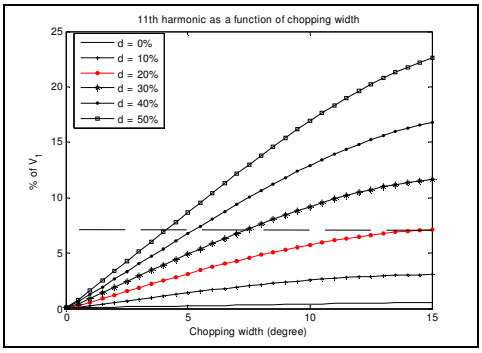
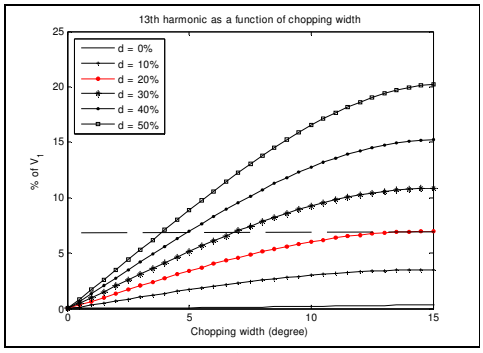


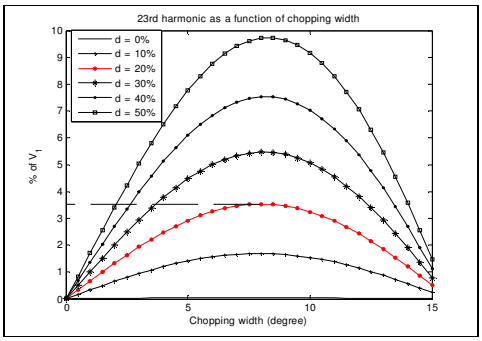
Figure D.1 Ideal Voltage Waveforms THD_V.


11th harmonic as a function of chopping width
d = 0%
d = 10%
d = 20%
d = 30%
d = 40%
d = 50%
% of V1
Chopping width (degree)

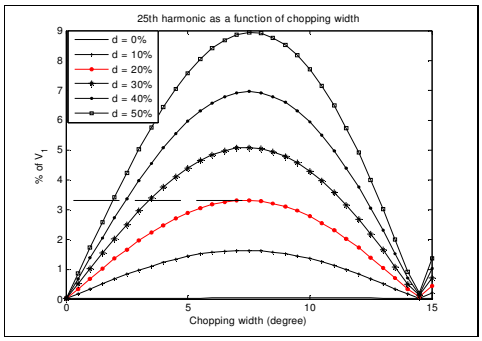
(a)


13th harmonic as a function of chopping width
d = 0%
d = 10%
d = 20%
d = 30%
d = 40%
d = 50%
% of V1
Chopping width (degree)

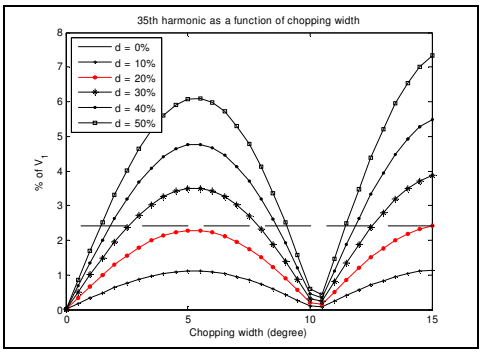
(b)


23rd harmonic as a function of chopping width
d = 0%
d = 10%
d = 20%
d = 30%
d = 40%
d = 50%
% of V1
Chopping width (degree)

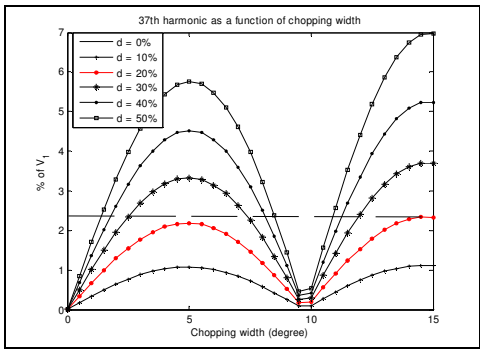
(c)


25th harmonic as a function of chopping width
d = 0%
d = 10%
d = 20%
d = 30%
d = 40%
d = 50%
% of V1
Chopping width (degree)

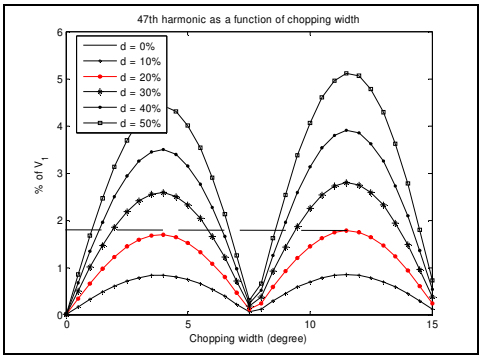
(d)


35th harmonic as a function of chopping width
d = 0%
d = 10%
d = 20%
d = 30%
d = 40%
d = 50%
% of V1
Chopping width (degree)

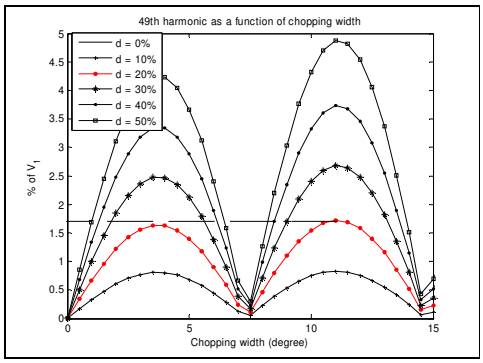
(e)


37th harmonic as a function of chopping width
d = 0%
d = 10%
d = 20%
d = 30%
d = 40%
d = 50%
% of V1
Chopping width (degree)

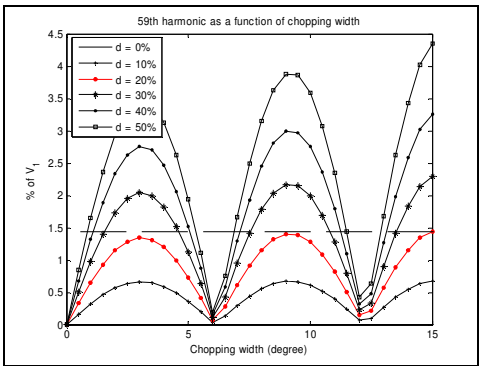
(f)


47th harmonic as a function of chopping width
d = 0%
d = 10%
d = 20%
d = 30%
d = 40%
d = 50%
% of V1
Chopping width (degree)

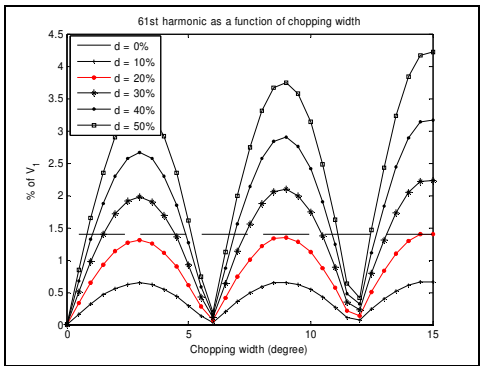
(g)


49th harmonic as a function of chopping width
d = 0%
d = 10%
d = 20%
d = 30%
d = 40%
d = 50%
% of V1
Chopping width (degree)

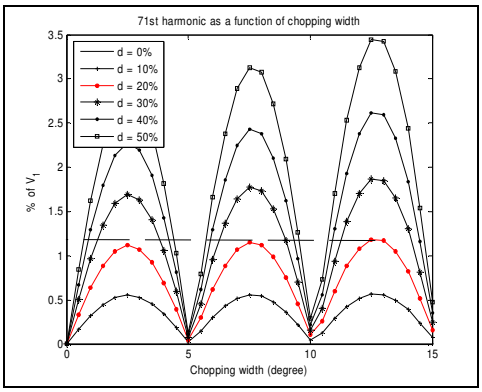
(h)



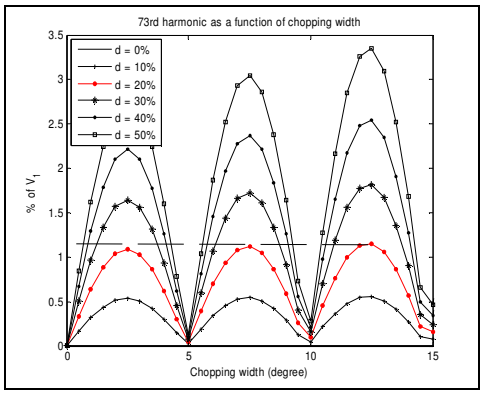
(i)



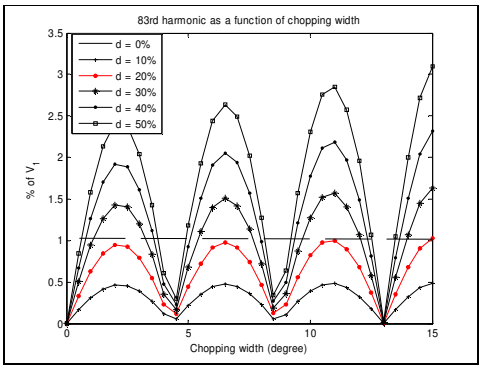
(j)



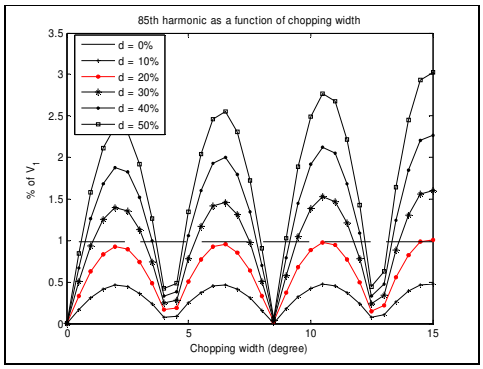
(k)



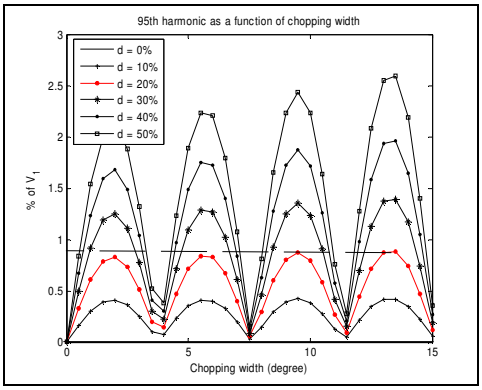
(l)



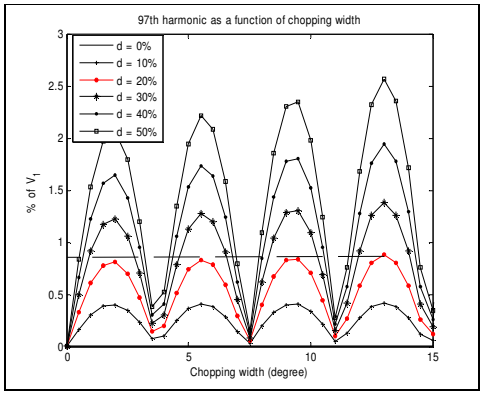
(m)



(n)



(o)



(p)

Figure D.2 Voltage Harmonic Components for Ideal Waveforms.

D.1.2 Current Harmonics

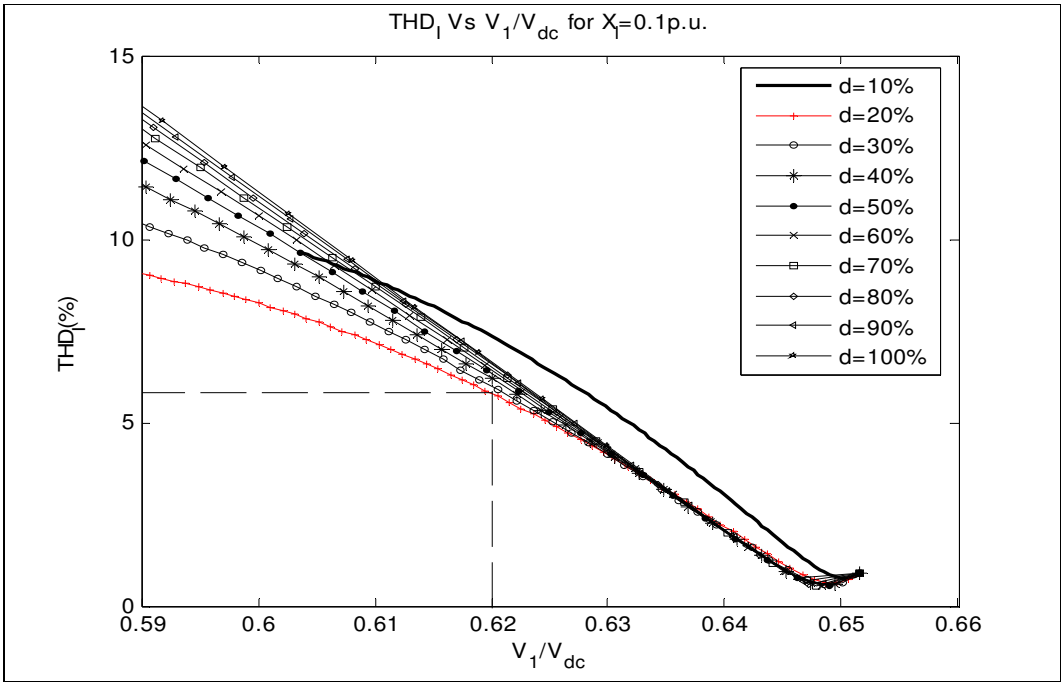


Figure D.3 Ideal Waveforms THD_I for x_l=0.1p.u.

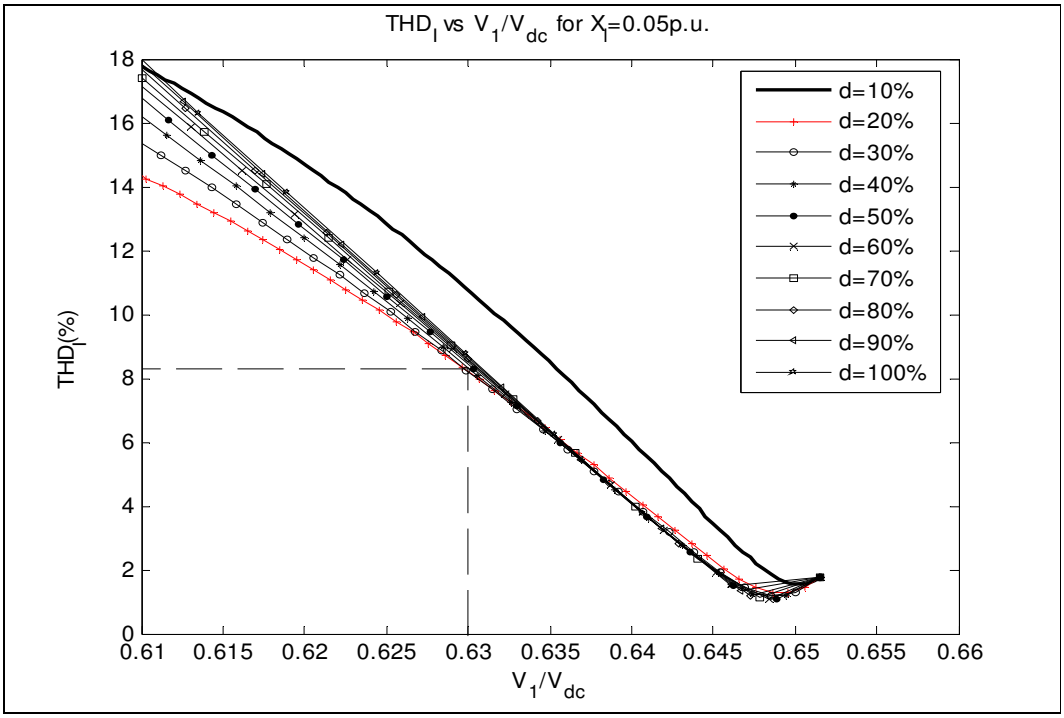
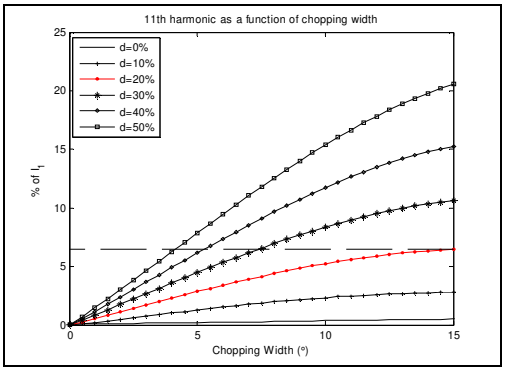
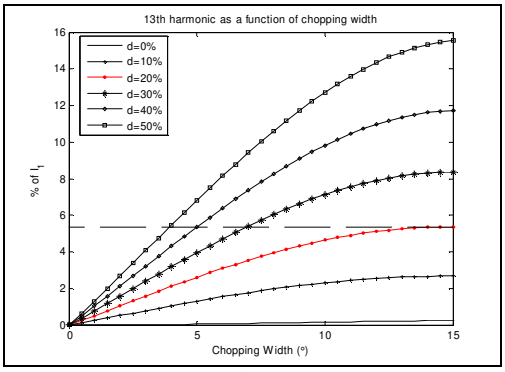


Figure D.4 Ideal Waveforms THD_I for x_l=0.05 p.u.

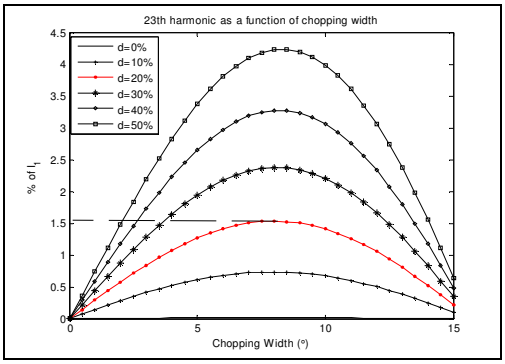
D.1.2.1 10% Interface Transformer Leakage Reactance



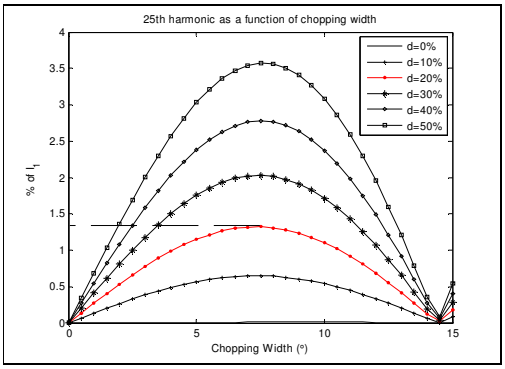
(a)



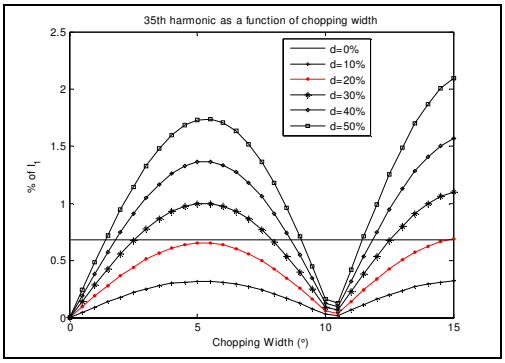
(b)



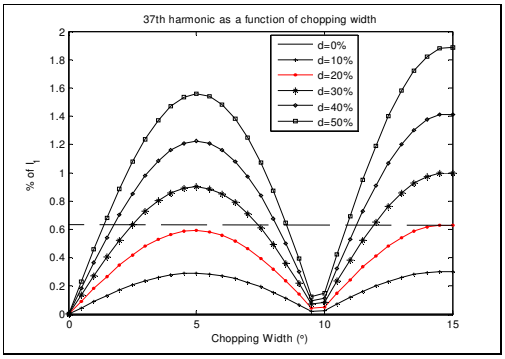
(c)



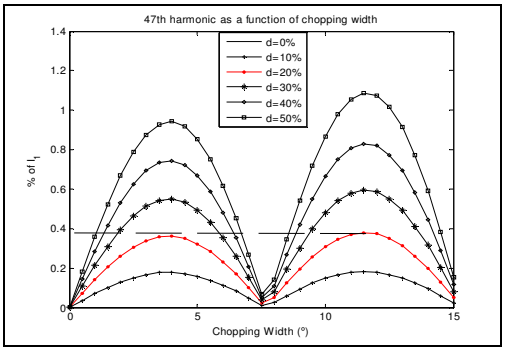
(d)



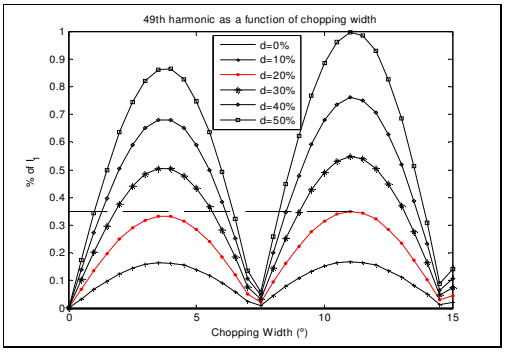
(e)



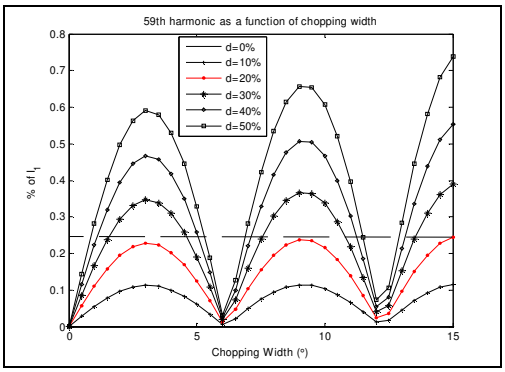
(f)



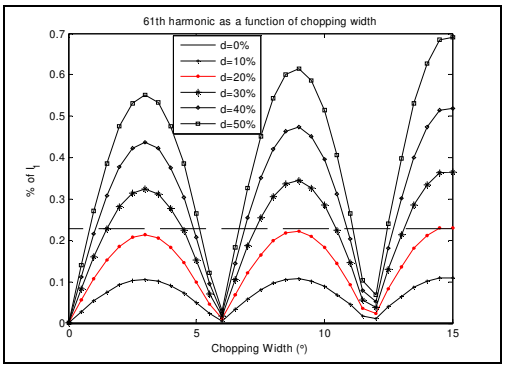
(g)



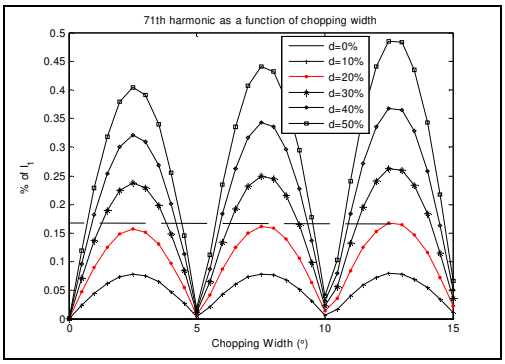
(h)



(i)



(j)



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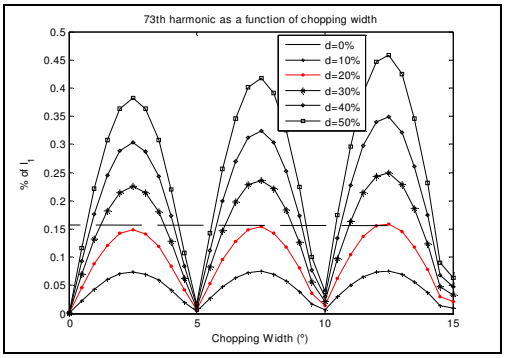

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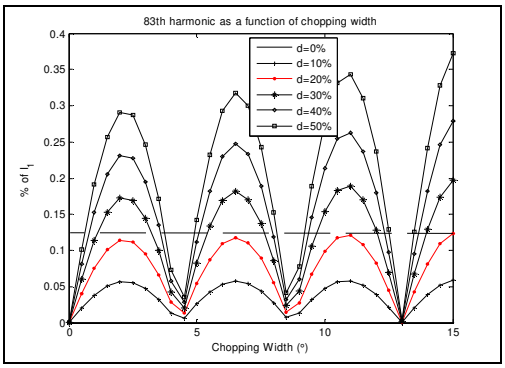

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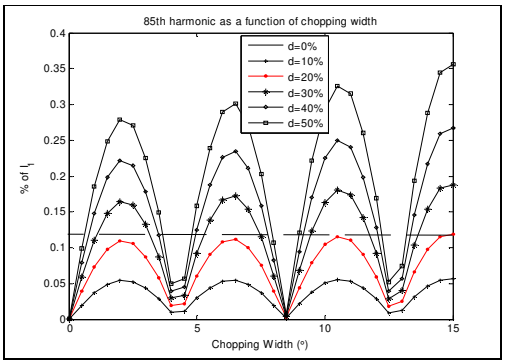

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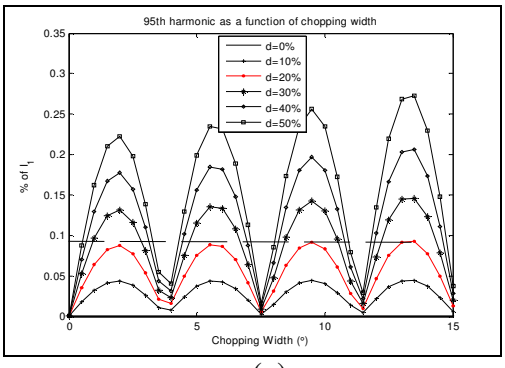

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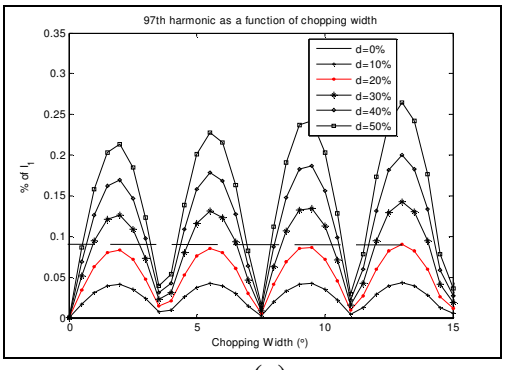

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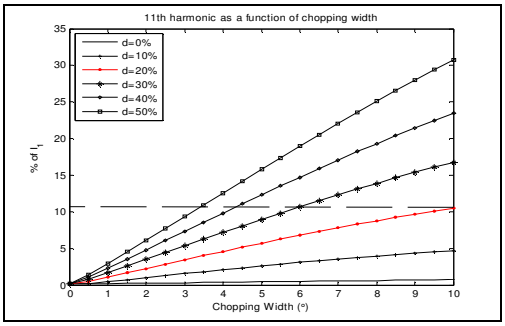
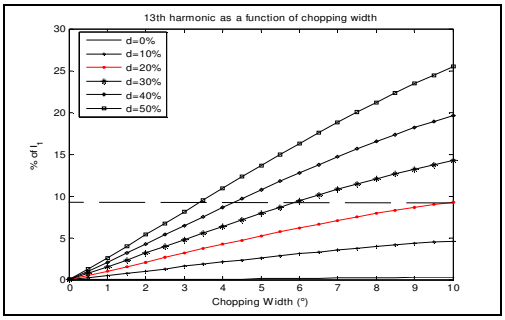
Figure D.5 Current Harmonic Components for Ideal Waveforms (10 % x_l)

D.1.2.2 5% Interface Transformer Leakage Reactance



(a)



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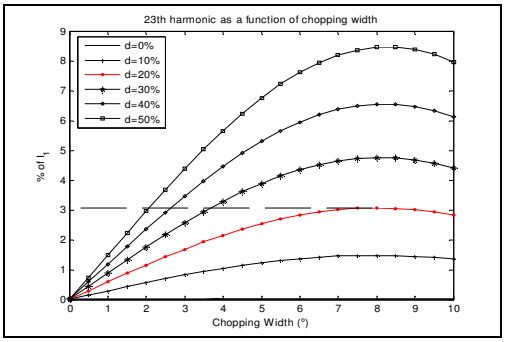

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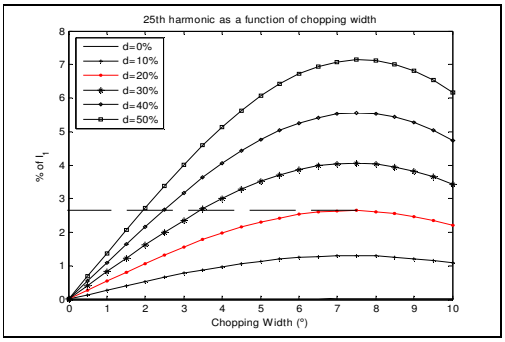
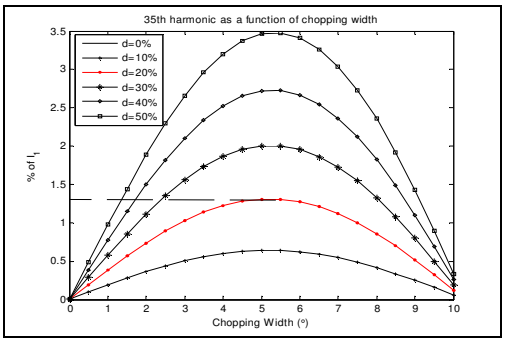
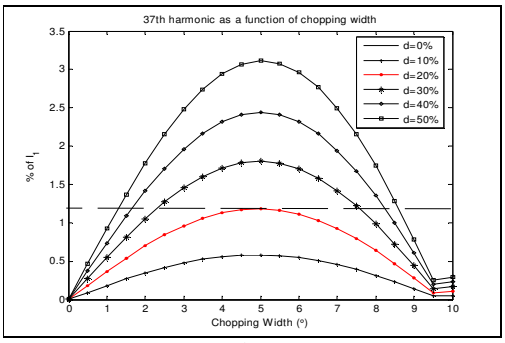


(d)



(e)



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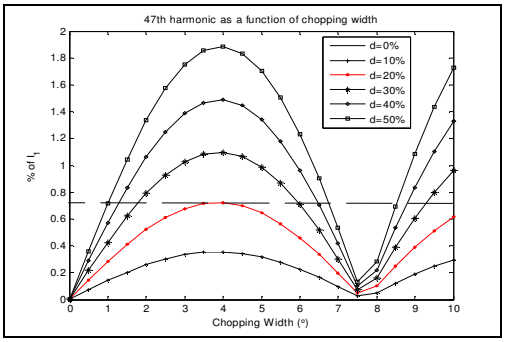
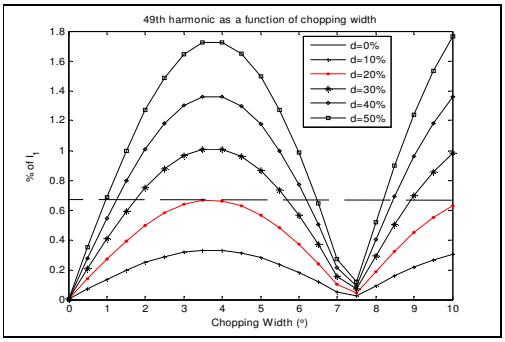


(g)



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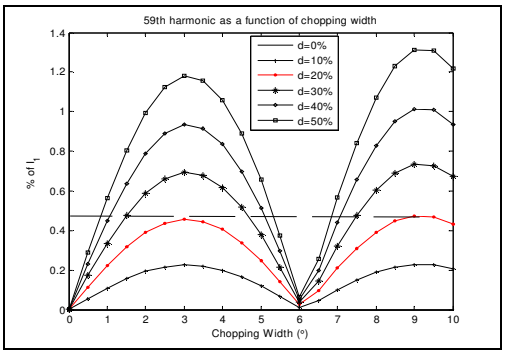

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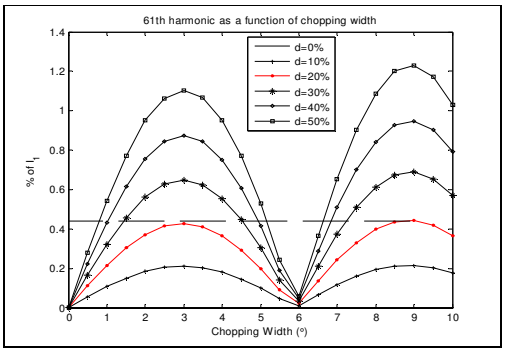

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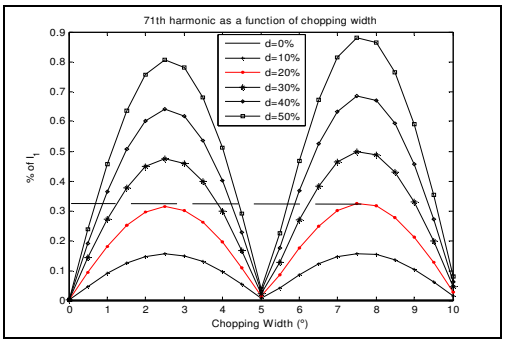

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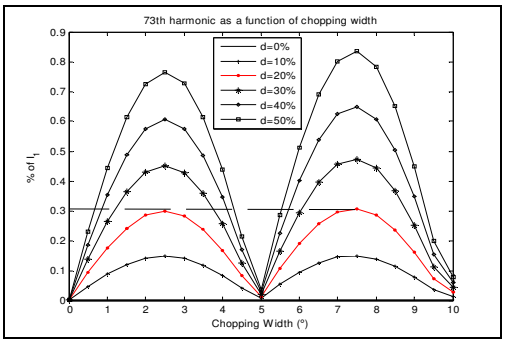

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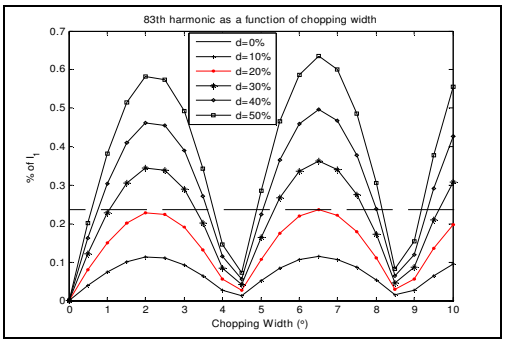

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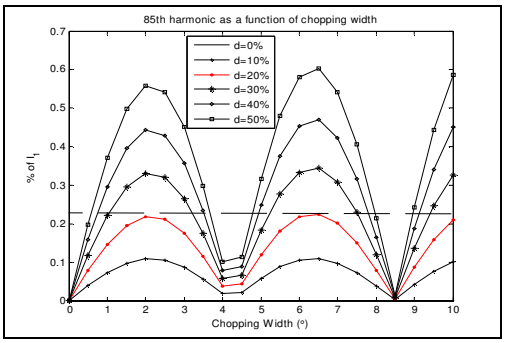

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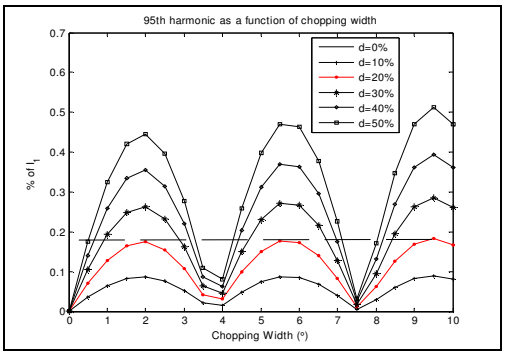

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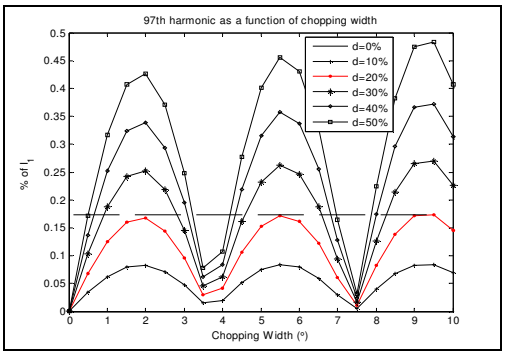
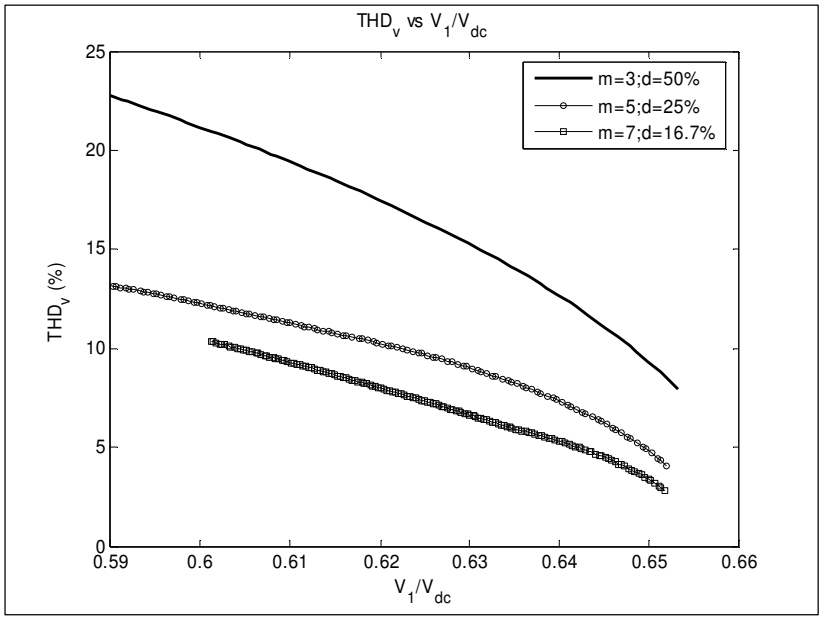


(p)

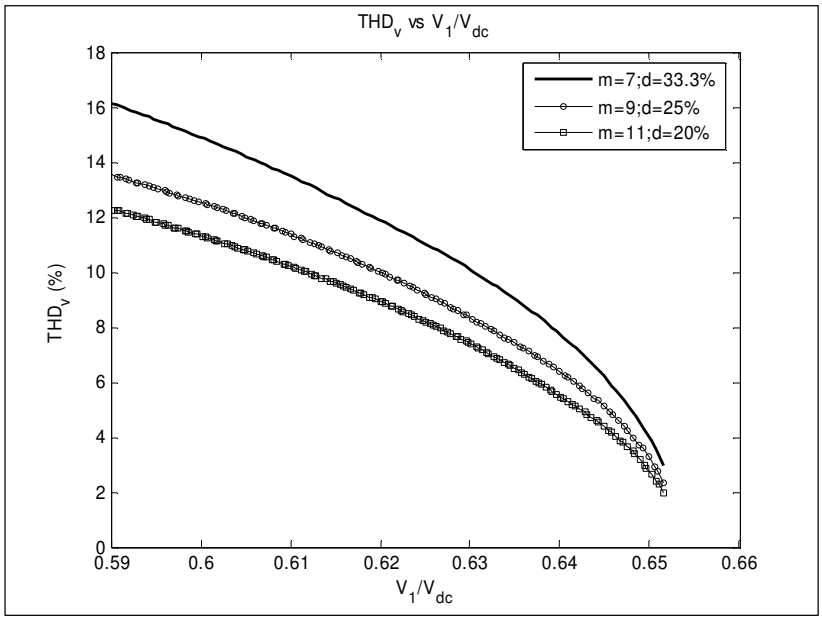
Figure D.6 Current Harmonic Components for Ideal Waveforms (5% x_l)

D.2 Stepped Waveforms

D.2.1 Voltage Harmonics



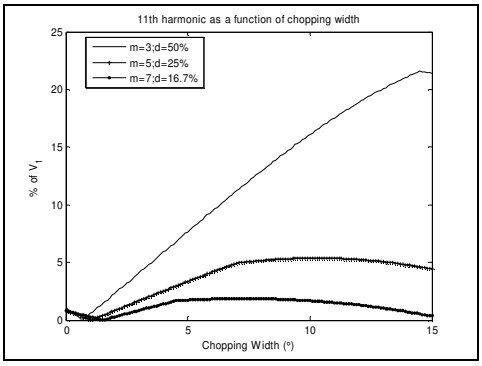
(a)



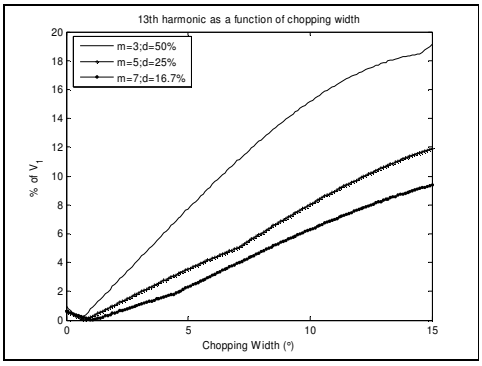
(b)

Figure D.7 1 and 2 Levels Notching THD_V.
(a) 1 Notching Level;
(b) 2 Notching Levels.

D.2.1.1 Harmonic Amplitudes for 1 Level Notching



(a)



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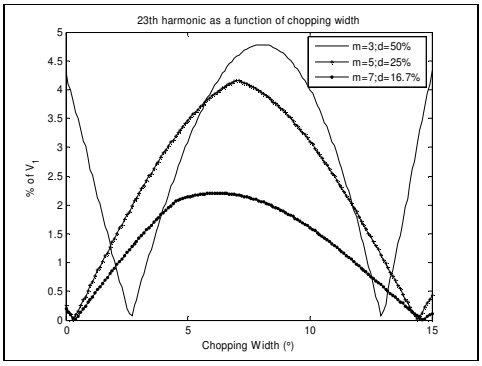

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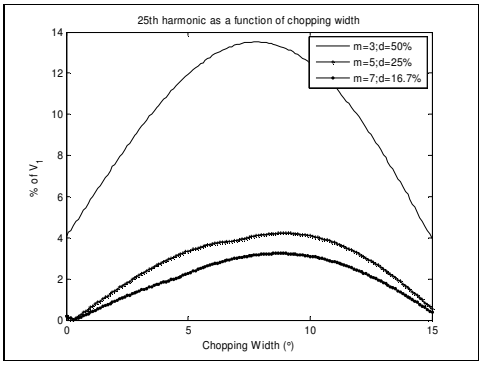

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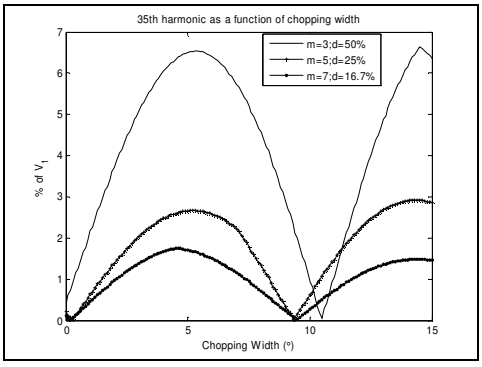

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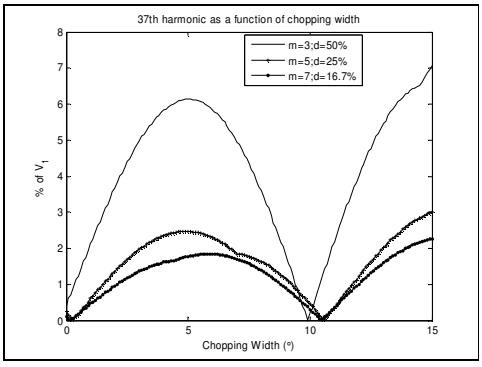

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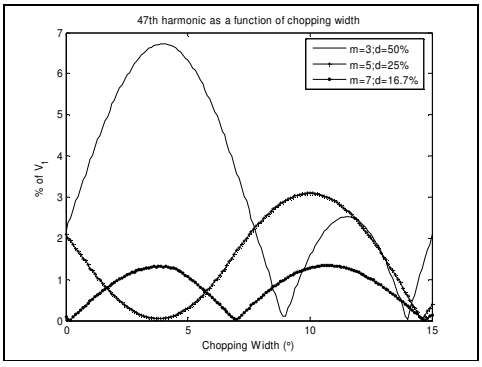
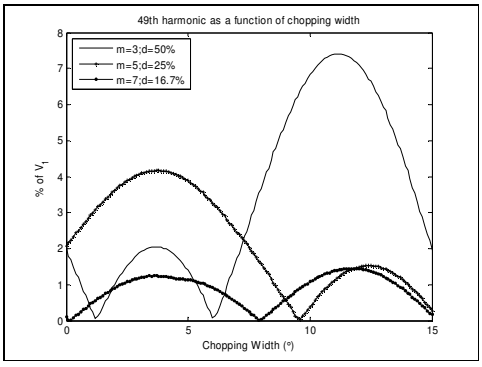


(g)



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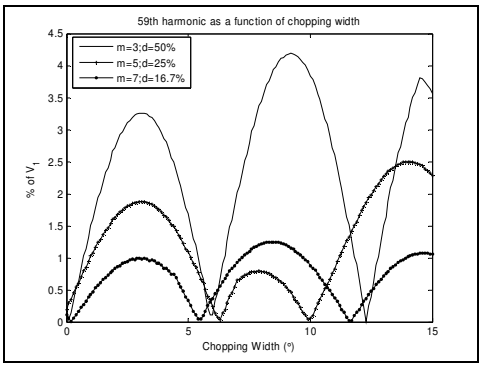

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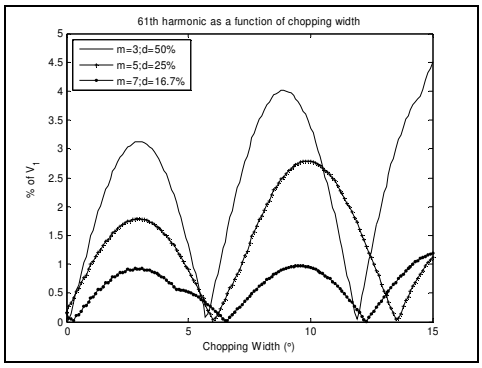

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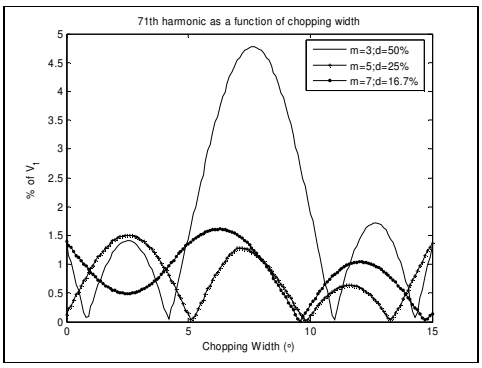
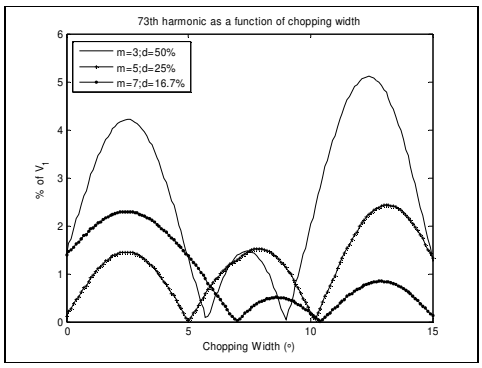


(k)



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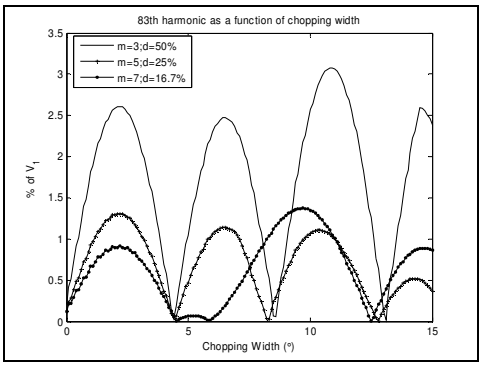
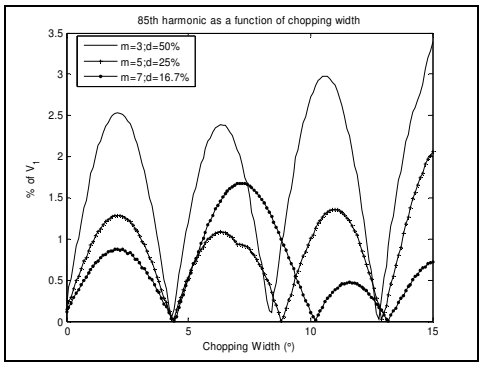


(m)



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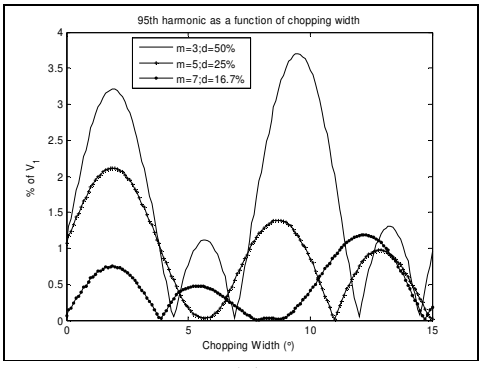

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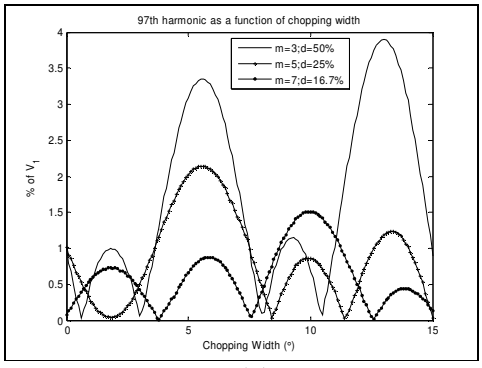

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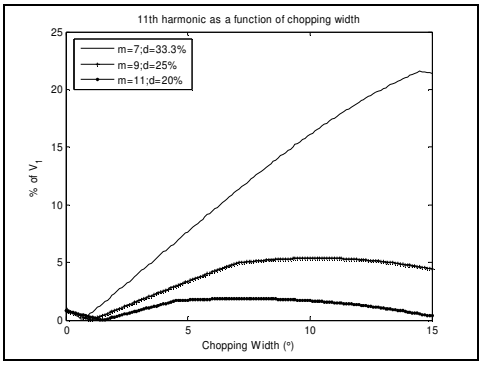
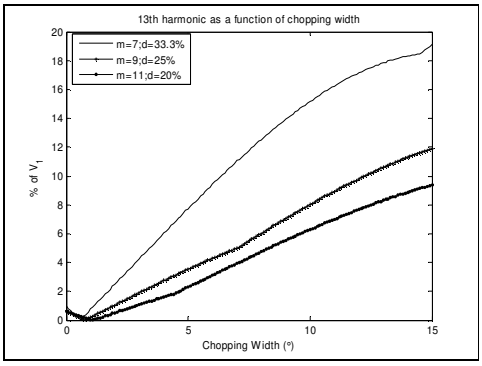
Figure D.8 Voltage Harmonic Amplitudes for 1 Level Notching.

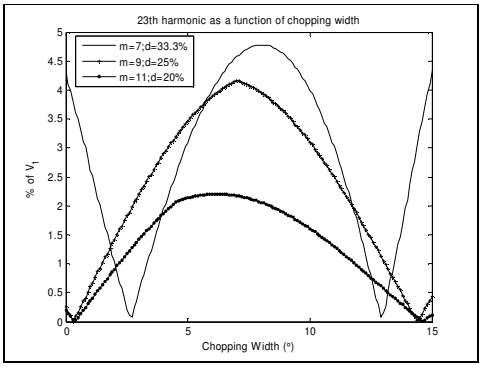
D.2.1.2 Harmonic Amplitudes for 2 Levels Notching



(a)



(b)



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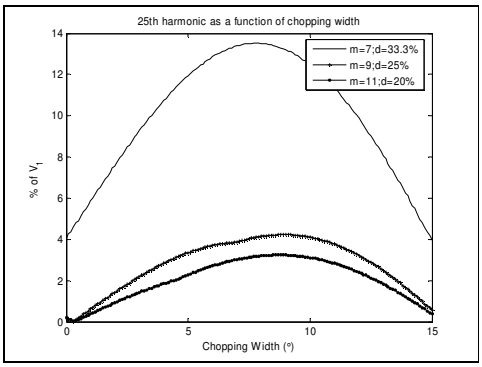
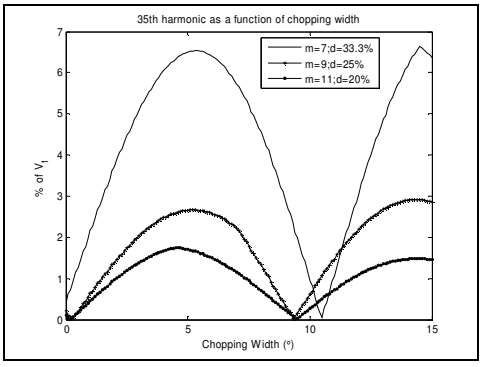


(d)



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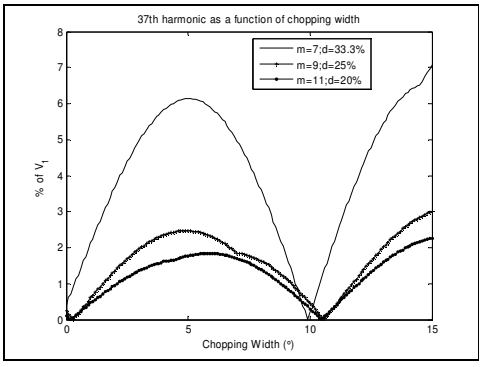

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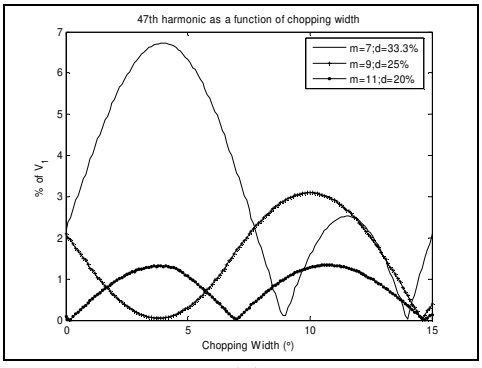

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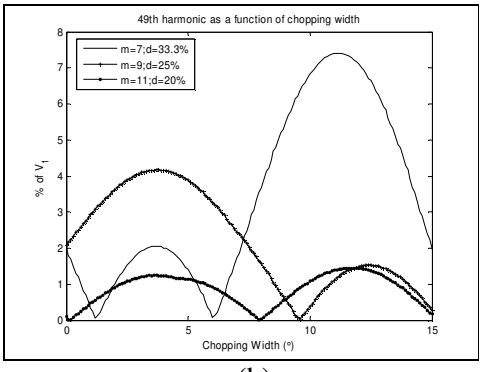

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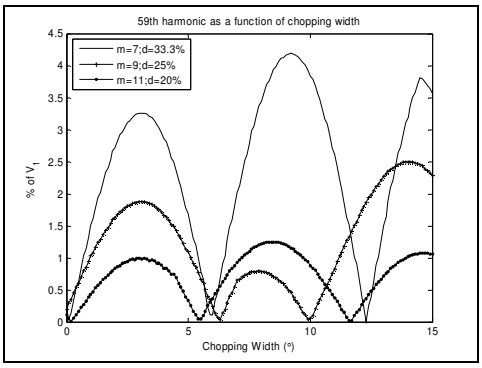

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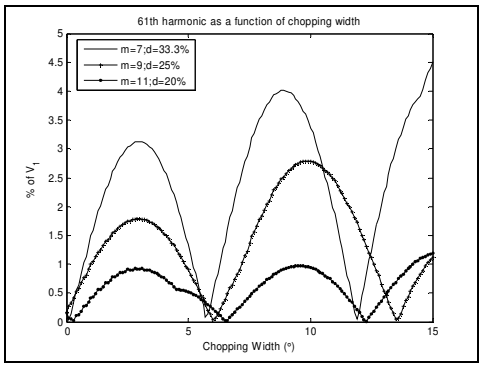

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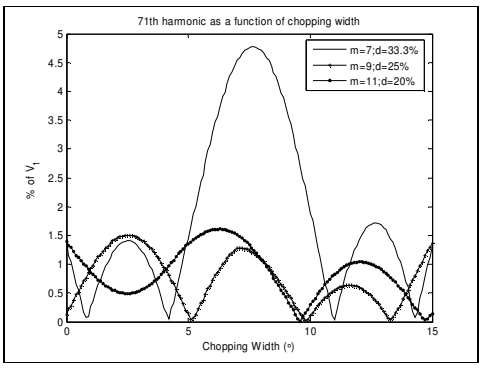

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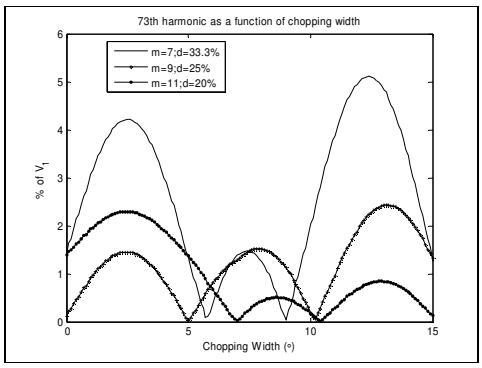

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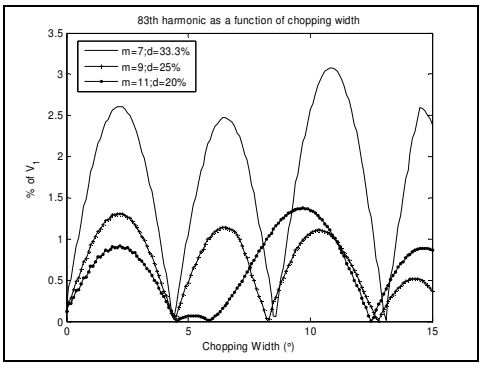

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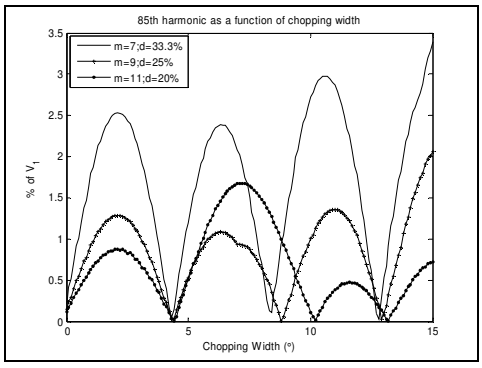

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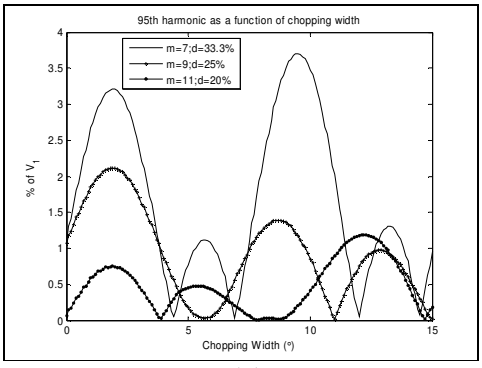

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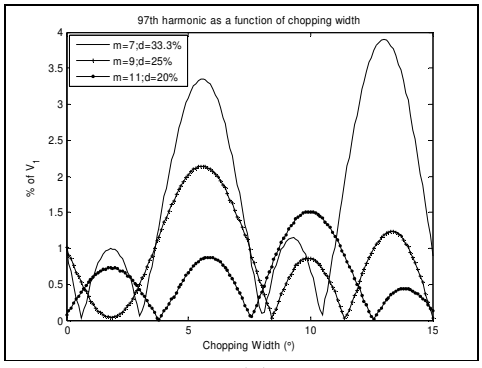

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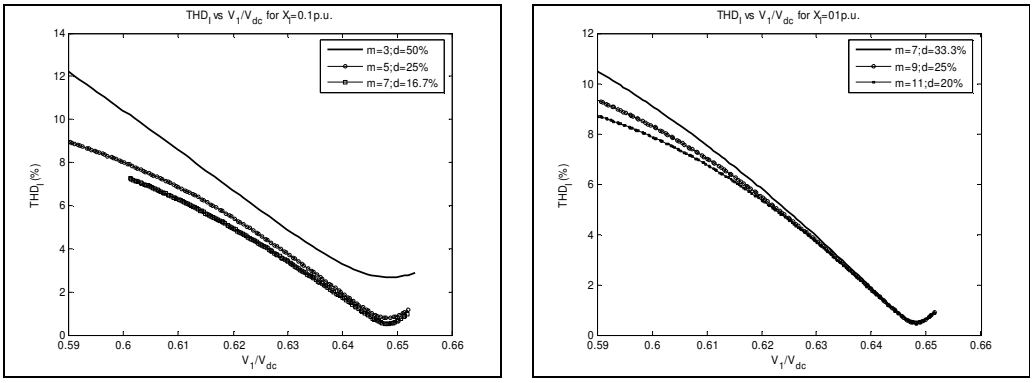
Figure D.9 Voltage Harmonic Amplitudes for 2 Levels Notching.

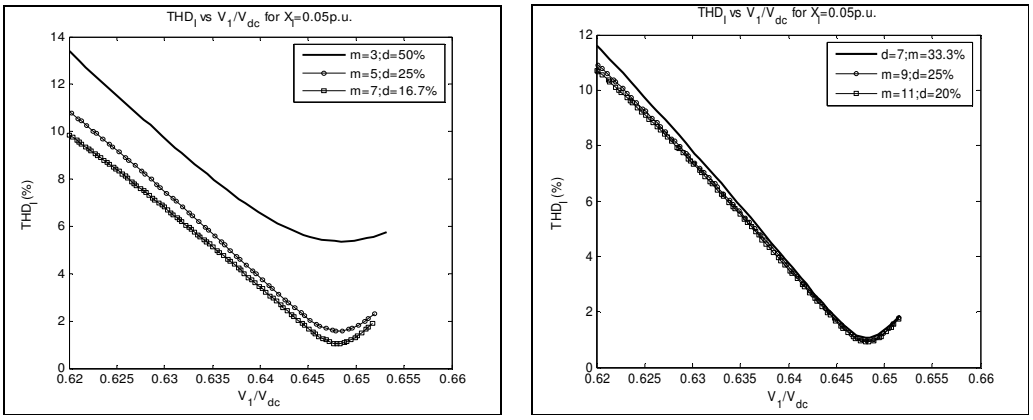
D.2.2 Current Harmonics



(a) (b)

Figure D.10 1 and 2 Levels Notching THD_I. (10% Interface Transformer Leakage Reactance, x_l)

(a) 1 Notching Level;
(b) 2 Notching Levels.

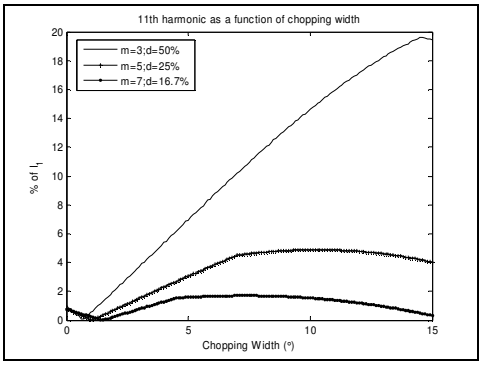


(a) (b)

Figure D.11 1 and 2 Levels Notching THD_I. (5% Interface Transformer Leakage Reactance, x_l)

(a) 1 Notching Level;
(b) 2 Notching Levels.

D.2.2.1 Harmonic Amplitudes for 1 Level Notching (10% x_l)



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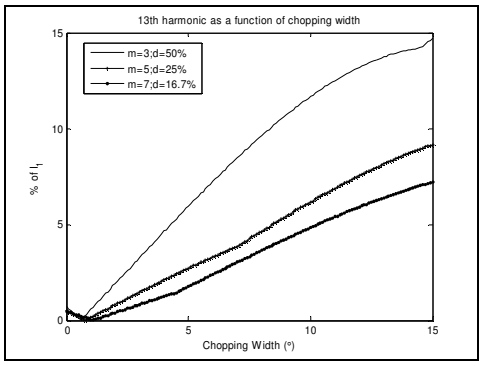

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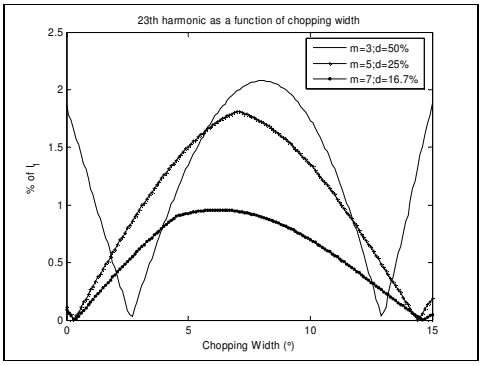

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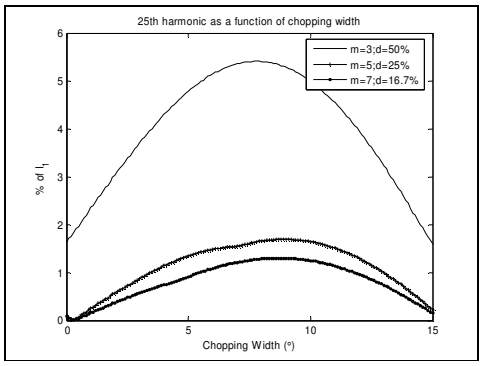

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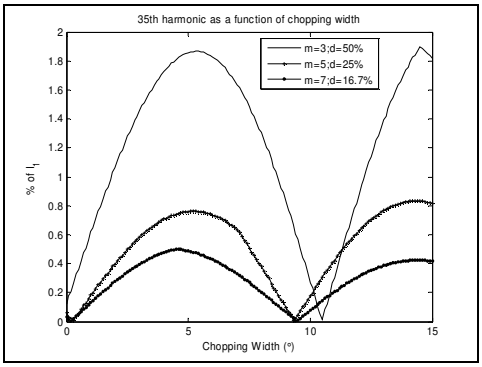

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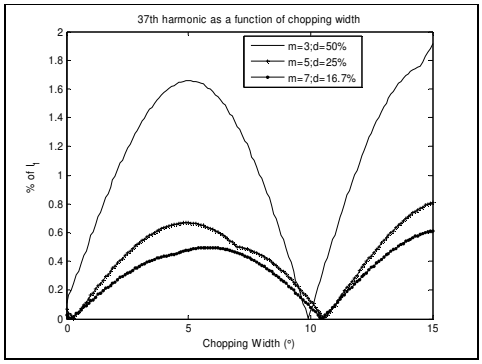

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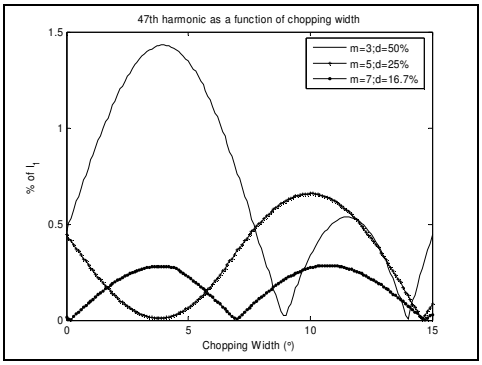

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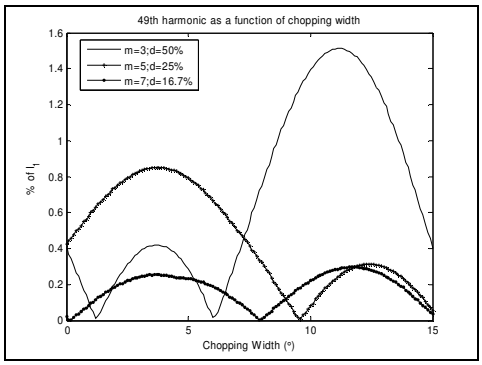

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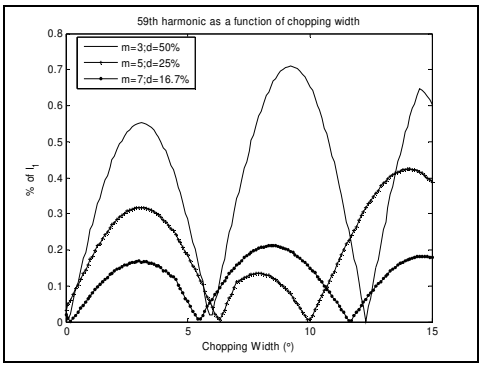

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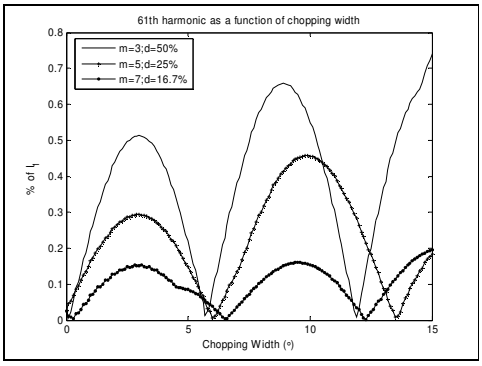

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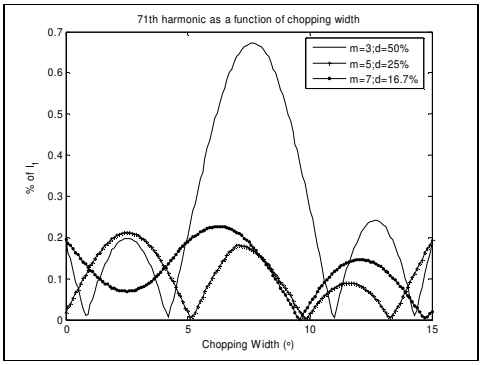

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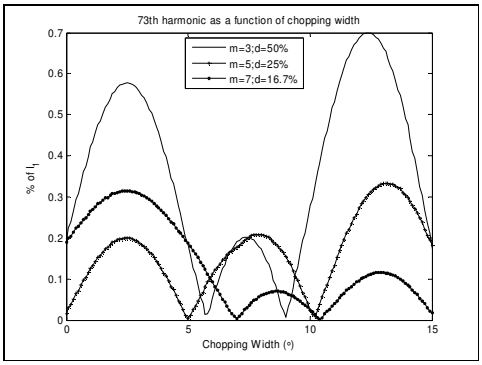

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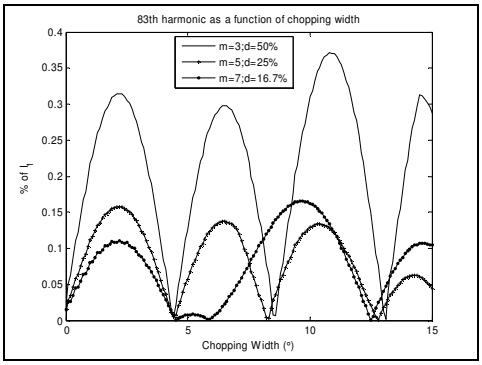

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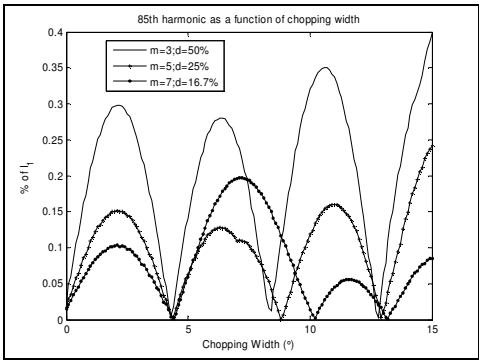

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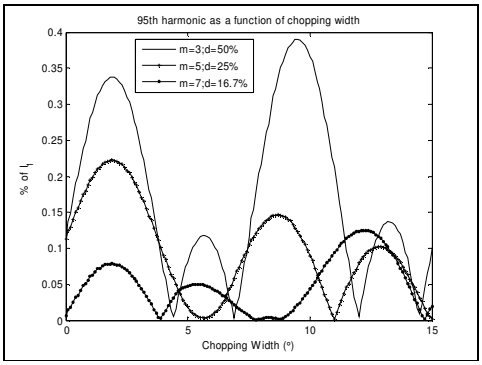

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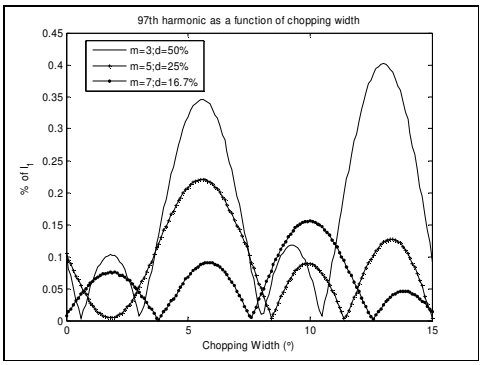

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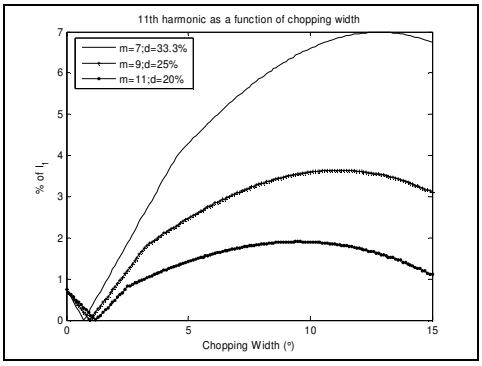
Figure D.12 Current Harmonic Amplitudes for 1 Level Notching (10% x_l)

D.2.2.2 Harmonics Amplitudes for 2 Levels Notching (10% x_l)



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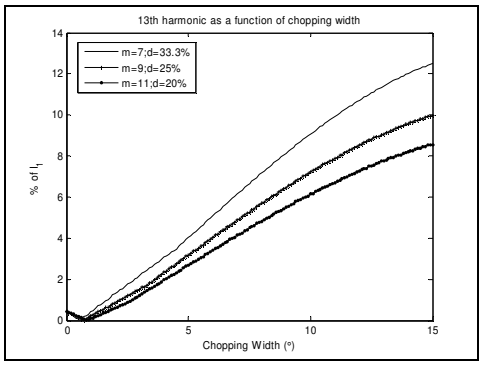

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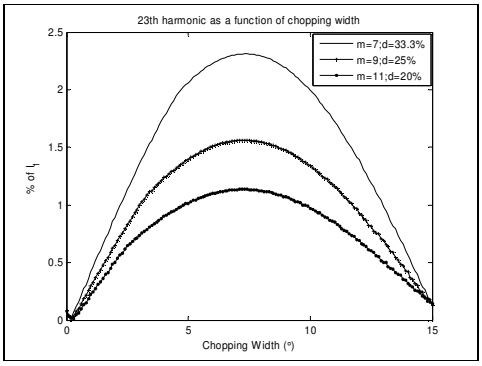

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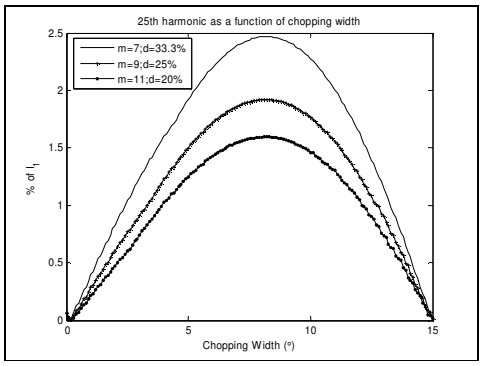

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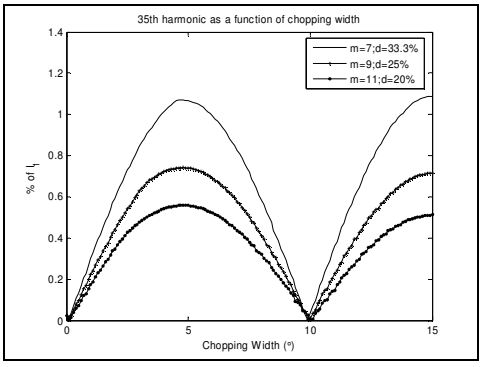

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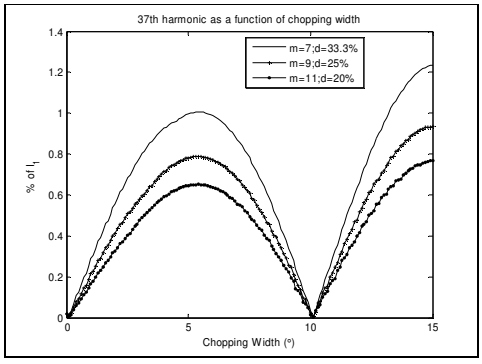

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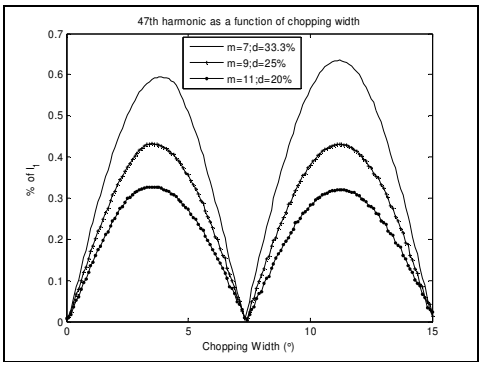

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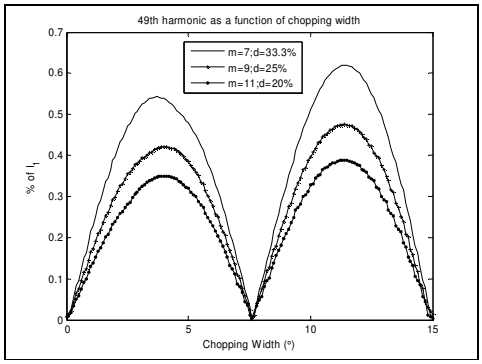

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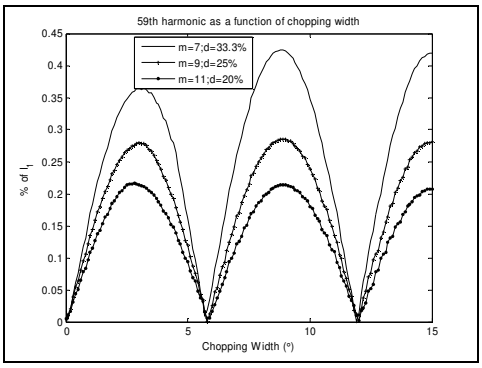

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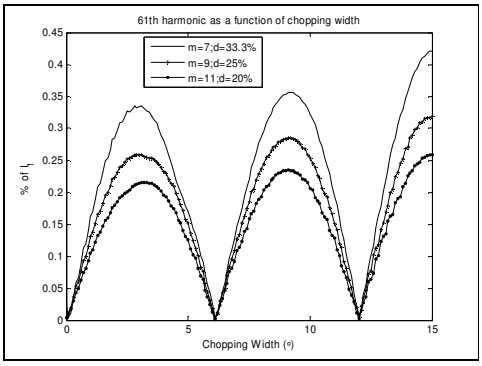

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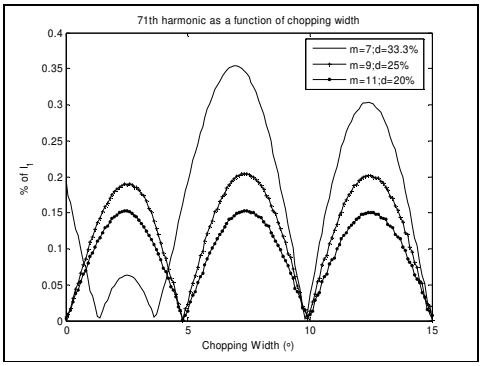

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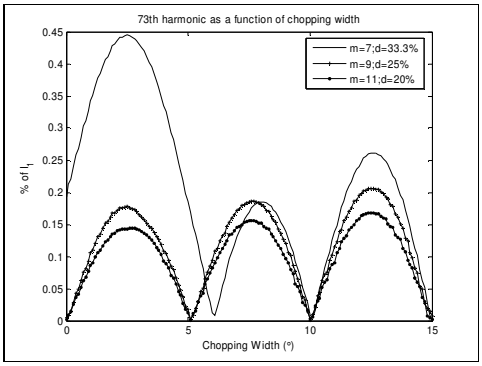

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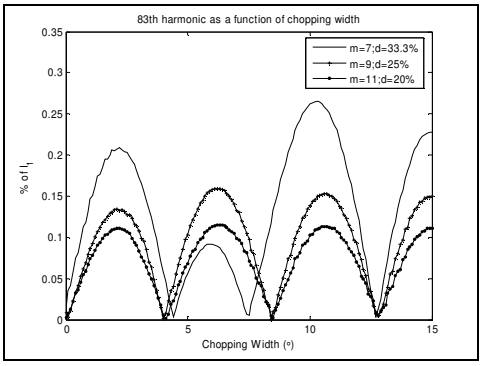

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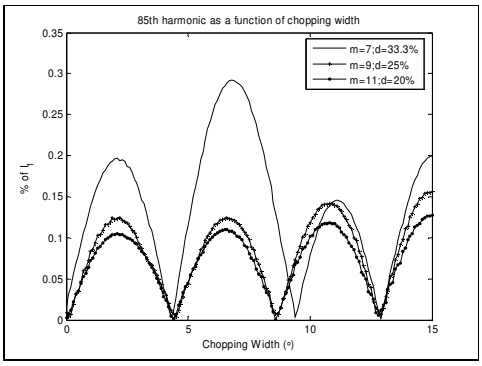

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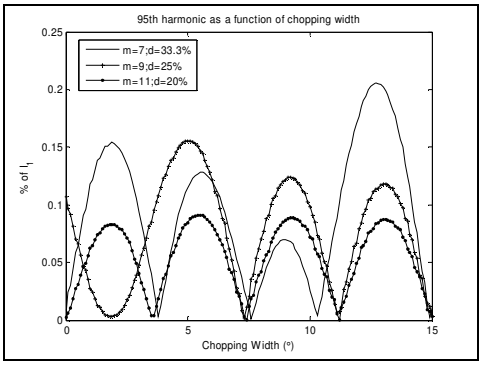

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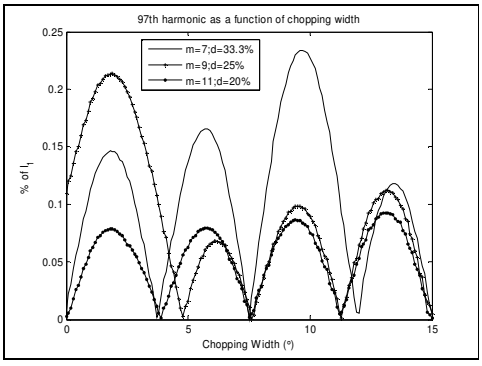

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Figure D.13 Current Harmonic Amplitudes for 2 Levels Notching. (10% x_l)

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